NORTHEAST ELECTRONICS
Division of nt northern telecom
Airport Rd., Concord, N.H. 03301•(603) 224-6511•TELEX 94-3453

INSTRUCTION MANUAL

MODEL 1260

PULSING TEST SET

PRINTED IN U.S.A.
2.5C-1260-0178
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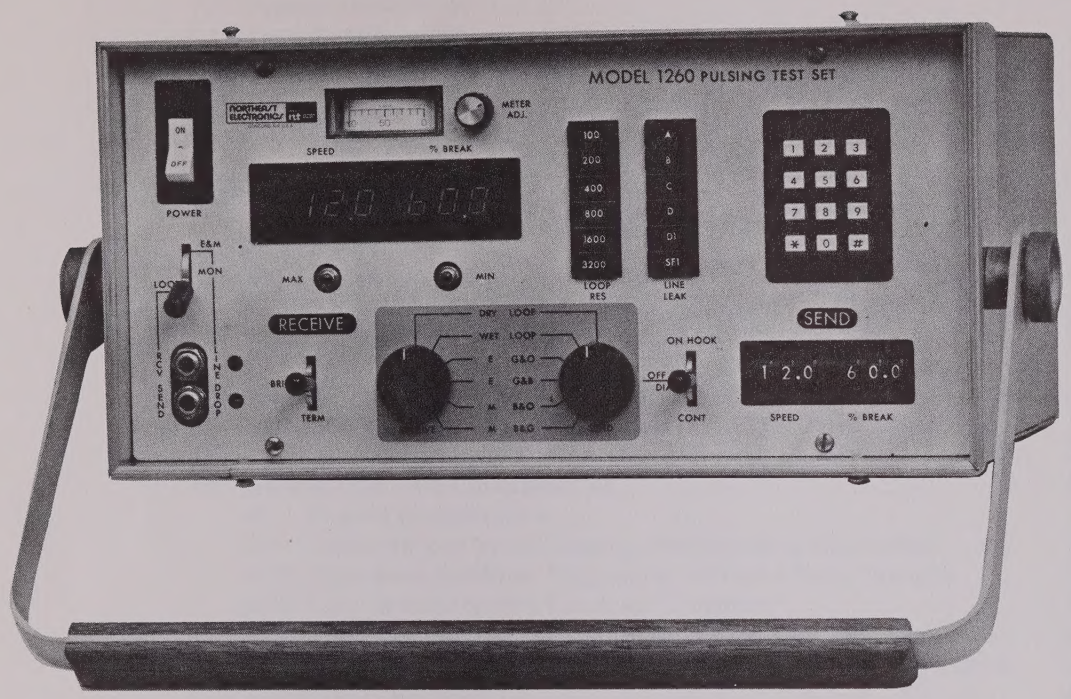

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SECTION 1

GENERAL DESCRIPTION

1.1 This manual describes the Northeast Electronics Model 1260 Pulsing Test Set. The test set is a precision digital instrument designed to send, receive, and measure pulsing in multiple loop and/or E&M modes. The sending and receiving capabilities are fully independent so mixed modes can be used . . . for example, sending loop while receiving E&M, or vice versa.

1.2 The send section can transmit continuous pulsing, or any number of dialing digits entered via a front panel keypad. Outpulsing speed and percent break are precisely variable over wide limits for testing of communications circuits and equipment over their ranges of operational performance requirements. Built-in loop resistance and line leak networks permit convenient loop simulation and margin testing as required.

1.3 The receive section automatically measures the speed and percent break of received pulsing. No premeasurement calibration is required. Measurement results are displayed on a digital readout.

1.4 The receive section can provide a 1260 user with all of the following speed and percent break measurement data:

- Averages over multiple pulses in a string;
- Minimums for individual pulses in a string (slowest speed and lowest percent break);
- Maximums for individual pulses in a string (fastest speed and highest percent break).

1.5 The minimum and maximum data helps reveal common signaling problems arising from individual pulse defects. These include: (a) first pulse problems from "A" relays, (b) split (double) pulsing and other erratic relay operations; (c) intermittent signaling conditions of other types.

1.6 The 1260 is designed such that continuously updated average measurement results appear on the digital readout with much the same "feel" as on an analog meter. A small analog meter is actually included on the front panel to enhance this effect. The meter directly indicates on and off hook status to show idle/busy conditions . . . and wink or delay dial conditions . . . plus short term percent break variations and longer term signaling dropouts. The meter indications are exactly the same for both loop and E&M operation.

1.7 TYPICAL APPLICATIONS

1.8 The Model 1260 is intended for pulse testing both signaling and switching equipment. It has the capabilities needed for:

- Acceptance testing of new plant;
- Routine and margin testing of in-service plant;
- Trouble sectionalizing;
- Alignment/tune-up adjustments.

1.9 The 1260's operating controls are arranged to simplify the task of exercising circuits over their ranges of sectional and end-to-end signaling requirements. Tests to margin limits for speed, percent break, leak, and loop resistance can all be performed using the 1260's built-in features.

1.10 The 1260 is also suitable for pulse testing/tuning a variety of signaling and switching components such as:

- Registers and senders;
- Pulse repeaters;
- Pulse correctors;
- Loop to/from E&M converters;
- Switch train components . . . digit absorbing selectors, regular selectors, connectors, and related equipment.

1.11 Dynamic testing can be performed on "A" relays under realistic conditions which closely approximate those existing in service.

1.12 TEST MODE SELECTION

1.13 The independent send and receive sections are each equipped to handle the following types of signaling arrangements:

- Dry loop;
- Wet loop, (battery and ground);
- E-lead ground and open;

- E-lead ground and battery;
- M-lead battery and open;
- M-lead battery and ground.

1.14 For wet loop pulsing, the 1260 makes/breaks both sides of the line. This is an important factor in some applications. A convenient test "A" relay, with 310 jacks to coil and contacts, is built into the 1260 and can be easily patch substituted for an in-circuit "A" relay whenever required by loop testing practices.

1.15 For E&M testing at 6-wire and 4-wire patch bays or other access points, the 1260's internal design makes it possible to easily select the proper leads for sending/receiving in either line or drop directions. Idle/busy status indicators and a reverse direction busyout feature are also built in for E&M testing.

1.16 **SEND SECTION**

1.17 A precision, crystal-controlled oscillator is the master reference for all outpulsing by the Model 1260. Outpulsing speed is variable from 1 to 29.9 pps in 0.1-pps steps. Percent break is variable from 10 to 89.9 percent in 0.1-percent steps.

1.18 Selected speed and percent break values apply to all outpulsing . . . whether continuous, or single-digit, or multi-digit. Selectable leak networks (normal, A, B, C, D, D1, SF1) and loop resistance (0 to 6300 ohms, 100-ohm steps) can also be imposed on outpulsing in loop modes.

1.19 **RECEIVE SECTION**

1.20 The speed of received pulsing is measured with accuracy of ± 0.1 pps over a range from 1 to 29.9 pps. The percent break of received pulsing is measured with accuracy of ± 0.5 percent over a range of 10 to 89.9 percent.

1.21 Fully accurate measurements can be made on digit "0" from a standard rotary dial. Average, minimum, and maximum measurement data can be displayed as desired.

1.22 Measurements can be made on a bridging basis or on a terminating basis.

1.23 **INPUT POWER**

1.24 The 1260 operates from -48 Vdc at 1 ampere maximum. Power is applied through a 310 jack in the rear of the unit. A combination on/off power switch, indicator light, and resettable circuit breaker is located on the front panel.

SECTION 2

SPECIFICATIONS

2.1 Table 2—1 is a list of specifications for the Model 1260 Pulsing Test Set.

Table 2—1. Model 1260 Pulsing Test Set Specifications

SEND SECTION	
Speed Range And Accuracy:	1 to 29.9 pps ±0.1 pps.
% Break Range And Accuracy:	10 to 89.9% break ±0.5 % break all modes except ±1% break for wet loop mode.
Loop Resistance:	0 to 6300 ohms in 100-ohm steps.
Line Leak:	A, B, C, D, D1 and SF1.
Send Relay:	Mercury-wetted contacts. Rated at 2 Amperes, internally fused at 1 Ampere.
Dial Keypad:	Can be used to outpulse at the speed and percent break set on the thumbwheels at a fixed interdigit time of 700 milliseconds.
RECEIVE SECTION	
Speed Range And Accuracy:	1 to 29.9 pps ± 0.1 pps.*
% Break Range And Accuracy:	10 to 89.9 % break ± 0.5 % break.*
Received Pulses Required:	At least 10 sequential pulses to obtain average speed and % break; At least 2 sequential pulses to obtain min/max speed and percent break.
Receive Input Circuit:	Termination, bridging, or an "A" relay coil.
"A" Relay Calibration:	Break gap: 0.006 in. Make gap: 0.004 in. Residual: 0.009 in. Readjust operate current: 16.5 mA Readjust non-operate current: 14.4 mA Dynamic test: 60 ± 2% break when pulsed at 60% break and 10 pps using leak A and 1200 ohms of loop resistance.‡
POWER INPUT:	42 to 57 Vdc at 1 Ampere maximum.

*Not measured through "A" relay.
‡Adjust spring tension until acceptable results obtained.

Table 2—1. (cont'd)

OPERATING ENVIRONMENT	
Temperature:	0° to 50°C (32° to 122°F).
Relative Humidity:	0 to 95% non-condensing.
DIMENSIONS:	14-1/4 in. w x 7-1/4 in. h x 12 in. d (without cover). 36.6 cm w x 18.4 cm h x 30.5 cm d. 14-1/4 in. w x 7-1/8 in. h x 14-1/8 in. d (with cover). 36.6 cm w x 18.1 cm h x 35.9 cm d.
WEIGHT:	20 pounds (9.1 kg).

SECTION 3

INSTALLATION

3.1 The Model 1260 is a portable test set and requires no installation.

3.2 INITIAL INSPECTION

3.3 The Model 1260 was carefully inspected, both mechanically and electrically, before shipment. It should be free of defects and should be operating correctly when received. To confirm this, the set sould be visually inspected for signs of damage that may have occurred during shipment. If there is shipment damage, notify the carrier immediately. Electrical operation can be quickly checked by following the self check procedure contained in Section 4.

3.4 RETURN MATERIAL AUTHORIZATION

3.5 As detailed on the back side of the sales agreement, Northeast Electronics warrants its instruments for a period of one year to the original purchaser. Before returning any piece of equipment to the factory for repair, a return material authorization number must be obtained from Northeast Electronics. To obtain this authorization, telephone the Customer Service Department at (603) 224-6511.

3.6 POWER CONNECTIONS

3.7 The test set operates from 48 Vdc office battery. Power connections are made via a 310 jack located on the rear of the set. Refer to paragraph 4.7 for details.

SECTION 4

OPERATION

4.1 INTRODUCTION

4.2 This section provides: (a) descriptions of individual controls, indicators, and jacks; (b) general considerations that apply to many different operating procedures; (c) detailed operating procedures.

4.3 CONTROLS, INDICATORS, AND JACKS

4.4 All operating controls shown on Figure 4—1 are described in Table 4—1.

NOTE

The "A" relay used in the Model 1260 was calibrated at the time of final test. It should be rechecked after shipment. For optimum results, recalibrate to user's specifications. Northeast Electronics specifications for the "A" relay are listed in Table 2—1.

Table 4—1. Model 1260 Controls, Indicators, And Jacks

REF DESIG	CONTROL, INDICATOR OR JACK	FUNCTION
	POWER SECTION	
A12J1	48V jack (rear panel)	310 jack for connection of central office battery. T = −48V, S = GND.
S1	POWER ON-OFF switch/ indicator/circuit breaker	When set to ON position, −48V is applied to unit and red indicator is lighted. When circuit breaker trips, switch is set to OFF position. The breaker is reset when placed at ON position.
	SEND SECTION	
S20	SEND mode switch	Selects indicated conditions to be used for signaling and pulsing at either J1 or J2.
S21	ON HOOK/OFF HK-DIAL/ CONT switch	In ON HOOK position, a continuous on-hook signal is applied to either J1 or J2. The actual signaling condition is determined by setting of SEND switch S20. In OFF HK-DIAL position, an off-hook signal determined by S20 is applied to either J1 or J2. When a digit is dialed on keypad, digit is outpulsed at speed and percent break set by S22 through S27. Interdigital time is 700 milliseconds. In CONT position, a continuous stream of pulses is applied to either J1 or J2. Make and break conditions are determined by S20 while speed and percent break are determined by S22 through S27.
S22, S23 & S24	SEND SPEED switches	Determine pulsing speed for continuous and dial modes. Can be set within range of 1 to 29.9 pps. Most significant digit cannot be set above 2. No pulses can be generated for numbers less that 1.

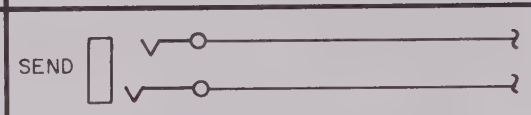
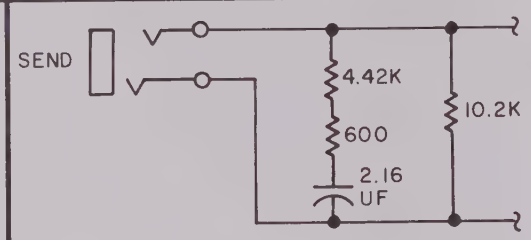
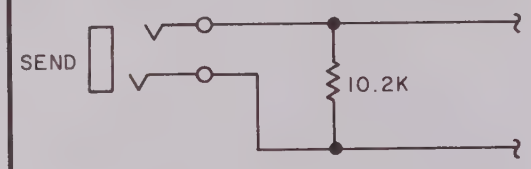
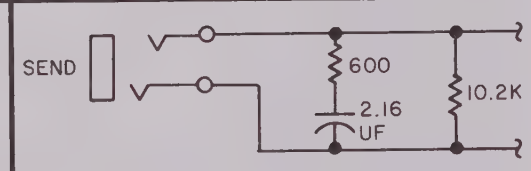
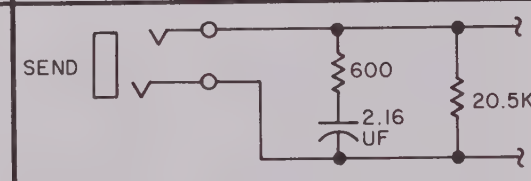
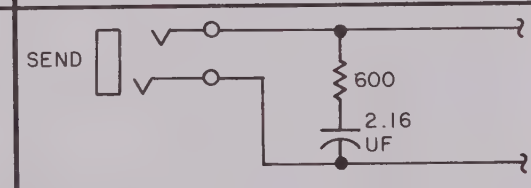
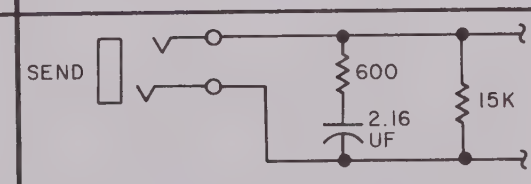
Table 4—1. (cont'd)

REF DESIG	CONTROL, INDICATOR OR JACK	FUNCTION
S25, S26 & S27	SEND % BREAK switches	Determine percent break for continuous and dial modes. Can be set within range of 10 to 89.9 percent break. Most significant digit cannot be set to either 0 or 9.
S17	Dial keypad	Controls digits to be outpulsed when S21 is in OFF HK-DIAL position. The * and # keys are inoperative.
S5 through S10	LOOP RES switches	Select value of balanced loop resistance placed in series with output when S20 is in either loop position. The switches are of the push-push type and select binary-weighted resistance values from 100 to 6300 ohms. When all switches are released, loop resistance is zero.
S11 through S16	LINE LEAK switches	Select either A, B, C, D, D1, or SF1 line leak conditions. Switches are mechanically interlocked so that only one switch at a time can be pushed. (See Table 4—2.)
RECEIVE SECTION		
S19	RECEIVE mode switch	Conditions receive section to accept signaling and pulsing as selected
S18	BRIDGE/TERM switch	When set to TERM position, the circuit under test is terminated in a low impedance of 400 ohms. When set to BRIDGE position, the circuit under test is bridged by a high impedance of 7K ohms.
S3 & S4	MAX and MIN pushbuttons	When both pushbuttons are depressed simultaneously receive section is reset and display is cleared. After at least 10 pulses have been received, average speed and percent break are displayed. When MAX pushbutton alone is depressed, displays maximum speed and percent break measured since the last time both pushbuttons were depressed at the same time. When MIN pushbutton alone is depressed, displays minimum speed and percent break measured since the last time both pushbuttons were depressed at the same time. NOTE When using either MAX or MIN pushbutton, although speed and percent break are displayed at the same time, it does not indicate that both occurred during the same pulse period.
U1 through U6	SPEED and % BREAK indicators	7-segment LED digital readouts that display speed and percent break measured by receive section.

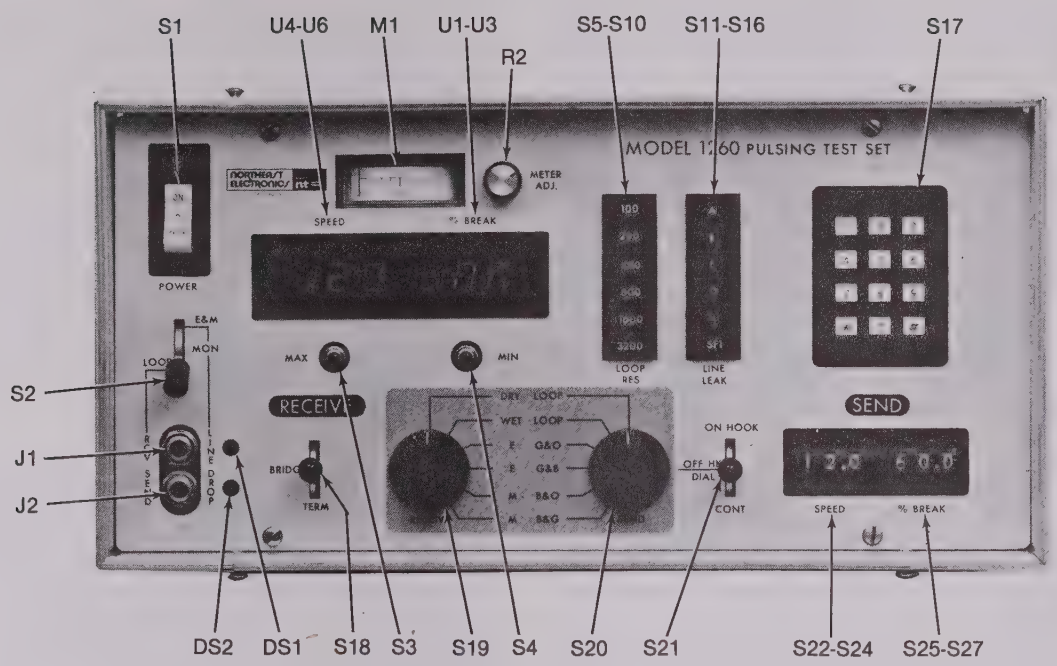
Table 4—1. (cont'd)

REF DESIG	CONTROL, INDICATOR OR JACK	FUNCTION
M1	Meter	Provides a gross indication of instantaneous percent break. Ends of scale also provide on-hook and off hook indications showing status of circuit under test.
R2	METER ADJ potentiometer	Allows meter percent break indication to be set to agree with the digital readout.
INPUT/OUTPUT JACKS, MONITOR INDICATORS AND CONFIGURATION CONTROL		
J1	RCV/LINE 310 jack	The input receive jack for loop pulsing when S2 is in LOOP position. The send/receive jack that looks toward the line when S2 is in E&M position.
J2	SEND/DROP 310 jack	The output send jack for loop pulsing when S2 is in LOOP position. The send/receive jack that looks toward the drop when S2 is in E&M position.
DS1 & DS2	Input/output jack monitor lamps	Indicate the signaling activity at J1 and J2 as controlled by SEND and RECEIVE switches S20 and S19 and configuration control switch S2. An on-hook condition is indicated by a lighted lamp and an off-hook condition by a lamp that is not lighted. When S2 is in MON position, upper lamp monitors the E lead at the tip of both jacks and the lower lamp the M lead at the ring of both jacks. When S2 is in either the E&M or LOOP positions, the lamps indicate what is being received and sent as controlled by S19 and S20.
S2	Input/output jack configuration control switch	When set to LOOP position, J1 and J2 are configured to be RCV and SEND jacks respectively for loop pulsing. When set to E&M position, J1 and J2 are configured to be LINE and DROP jacks respectively. When set to MON position, the tip and ring of J1 are connected to the tip and ring of J2 and the unit monitors the traffic on the E and M leads.
"A" RELAY SECTION		
A12J2 & A12J3	"A" RELAY 310 jacks (rear panel)	A pair of jacks for access to "A" relay coil and contacts. J3 is COIL jack and J2 the CONTACTS jack.

Table 4—2. Line Leak Networks

LEAK	SCHEMATIC	SIMULATES
NONE		Open circuit.
A		A subscriber line near the central office equipped with 5 C4A ringing bridge extensions and a 15,000-ohm leak on the drop wire.
B		A sender output without contact protection and with a 10,200-ohm leak.
C		A circuit sender loop pulsing network with a 10.2 K ohm leak across the trunk.
D		A sender output with a leak of 20,500 ohms.
D1		Normally used with dial pulse sender circuits for loop pulsing to improve the percent break at the distant selector or connector "A" relay contacts.
SF1		A sender output with a 15,000-ohm leak.

B01421



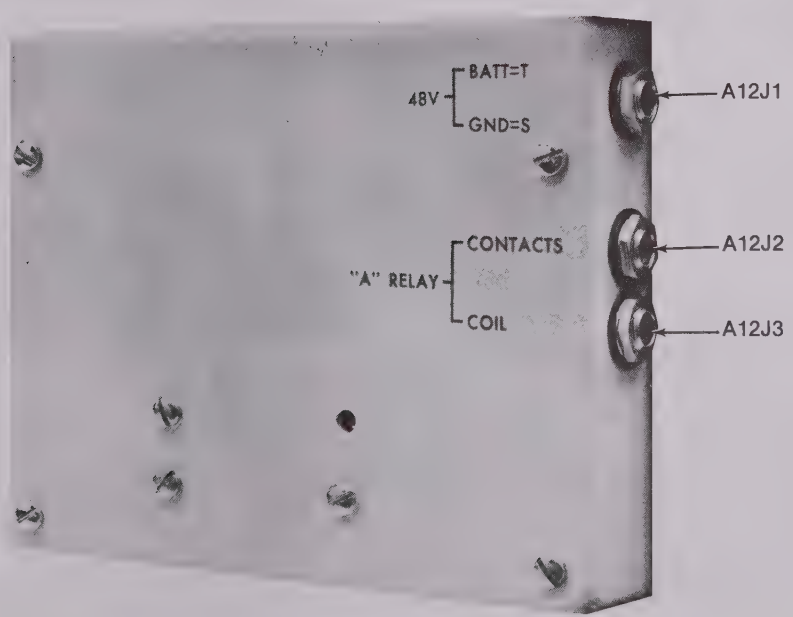


Figure 4—1. Model 1260 Controls, Indicators, And Jacks

4.5 GENERAL OPERATING CONSIDERATIONS

4.6 Paragraphs 4.7 through 4.23 contain a set of general operating considerations that are referenced throughout the more detailed operating procedures contained in paragraphs 4.24 through 4.41.

4.7 POWER CONSIDERATIONS

4.8 The Model 1260 is designed to operate from a central office supply within the range of 42 to 57 Vdc. The maximum load current is 1 Ampere. A 310 jack mounted on the rear panel of the unit is used for input power connections. Connect −48 Vdc to the tip and ground to the sleeve. The length of the power cord from the central office supply to the Model 1260 must not exceed 10 feet.

4.9 CONSIDERATIONS WHEN SENDING AND RECEIVING DIAL PULSES

4.10 When measuring pulsing speed and percent break of dialed digits, the average, minimum, and maximum digital readout indications depend upon certain conditions. These conditions include the actual digits dialed and the interdigital time. The normal method of operating the Model 1260 for measuring dialed digits is to: (a) dial a digit, (b) measure and display it on the Model 1260, and (c) then depress the MAX and MIN pushbuttons simultaneously to clear the digital displays before measuring the next digit. This minimizes any possibility of obtaining erroneous readings.

4.11 The Model 1260 requires a minimum of 10 consecutive pulses to generate an average display. Thus, when dialing digits to be measured by the Model 1260, dial the numeral 0 in order to obtain an average digital readout. If consecutive zeros are dialed, the digital readout will be updated each time a digit is measured. This assumes that an interdigital time of at least one second is always used. There will be no average digital readout for any digits other than 0.

4.12 The Model 1260 will display valid minimum and maximum readouts for any digit from 2 through 0 whenever either the MAX or the MIN pushbutton is depressed. These readouts are updated for each pulse that is measured providing the speed or percent break is: (a) greater than the previous maximum or (b) less than the previous minimum since the last time both pushbuttons were depressed simultaneously. When pulsing digits 2 through 9 that are to be measured by a Model 1260, ensure that the interdigital time is at least one second. Otherwise erroneous minimum and maximum readouts will occur.

4.13 CONSIDERATIONS WHEN DIAGNOSING INDIVIDUAL PULSE PROBLEMS

4.14 A particularly useful application of the min/max function is that of detecting first pulse problems in relays and other relay-type equipment such as switch trains. When this type of problem exists, the percent break of the first pulse in a dialed digit may be decreased to the point where the call is completed to the wrong number or maybe not be completed at all. The same type of problem can also occur regularly during some pulse other than the first pulse. In either case, the Model 1260 can be used to pinpoint the problem to a given pulse in a digit, provided the problem occurs on a regular enough basis to allow solid confirmation. This is possible because the Model 1260 can display the minimum percent break measured in any digit from 2 through 0.

4.15 To confirm a suspected first pulse problem, clear the 1260's display and pulse the circuit under test with the digit 0. After a digital display appears, depress the MIN pushbutton. If a first pulse fault did occur, the minimum percent break will be considerably less than the percent break selected on the pulsing test set. Next clear the display again and pulse the circuit with the digit 2. Again depress the MIN pushbutton. If the minimum percent break is again very low, it is confirmation that the percent break of the first pulse is being distorted. If the minimum percent break displayed is normal, this indicates that the percent break is being distorted during a pulse other that the first. The pulse at fault can be detected using the technique outlined in paragraph 4.16. The tests just described should be repeated a number of times to determine if the problem is chronic or intermittent.

4.16 When the minimum percent break from a measured 0 is very low but is not a first pulse problem, the pulse in error can be located by sequentially measuring and displaying the digits 2 through 9 until the minimum percent break is found to be very low at a particular digit. The pulse having the distorted percent break is then known to be one digit less than the digit that produced the abnormally low minimum percent break. For example, assuming the digit 0 produces a low minimum percent break; the digit 4 is normal, and the digit 5 is a low minimum percent break; it can then be deduced that the fourth pulse has a distorted percent break. Between digits, reset the display by depressing the MAX and MIN pushbuttons simultaneously. This procedure should be repeated a number of times to determine whether the problem is chronic or intermittent.

4.17 LOOP RESISTANCE AND LINE LEAK CONDITIONS

4.18 The loop resistance and line leak conditions are used in the send mode for dry loop or wet loop pulsing only. Resistance values of zero to 6300 ohms can be selected in 100-ohm increments. This is used to simulate the copper resistance offered to pulsing circuits.

4.19 Standard leak conditions of A, B, C, D, D1, and SF1 can be selected. Refer to Table 4—2 for the schematic diagrams of the leak circuits provided in the Model 1260.

4.20 USING THE SEND MODE SWITCH TO SUPPLY E&M BUSY SUPERVISION

4.21 When sending in any of the E&M modes, positioning of the SEND mode switch automatically busies out the appropriate lead in the reverse direction. When receiving in any of the E&M modes, the SEND mode switch can be set to busy out the appropriate lead in the reverse direction. Refer to Tables 4—3 and 4—4 for the correct combinations of switch settings.

4.22 MEASUREABLE COMBINATIONS OF PULSING SPEED AND PERCENT BREAK

4.23 There are certain combinations of pulsing speed and percent break that the Model 1260 cannot measure. These occur at both the highest and lowest extremes of percent break when using the highest allowable pulsing speed. Figure 4—2 shows a graphical representation of the interrelationship of these parameters. The area enclosed by the graph defines the measureable combinations of pulsing speed and percent break. Any combination that falls outside of the enclosed area will not generate any type of digital readout on the Model 1260.

4.24 **OPERATING PROCEDURES**

4.25 Paragraphs 4.28 through 4.41 provide operating procedures for using the Model 1260 in all of its send only, receive only, send and receive simultaneously, and mixed-mode operations such as sending loop and receiving E&M. Paragraph 4.26 is a self check that can be performed at any time to verify that the unit is operating properly.

Table 4—3. Busy Conditions When Sending E&M

SEND Switch S20	Configuration Switch S2	Jack/Lead Busied
E G&O or E G&B	E&M	J1 LINE, M Lead = Resistance Battery
M B&O or M B&G	E&M	J2 DROP, E Lead = GND

Table 4—4. Busy Conditions When Receiving E&M

Configuration Switch S2	RECEIVE Switch S19	SEND Switch S20	Jack/Lead Busied
E&M	E G&O or E G&B	Either M position	J2 DROP, E Lead = Gnd
E&M	M B&O or M B&G	Either E position	J1 LINE, M Lead = Resistance Battery

4.26 SELF CHECK

4.27 To check out the receive and send sections, perform the following steps.

1. Insert a 310 plug into the 48V jack on the 1260 rear panel.

2. Connect the other end of the power cord to central office battery and ground. Refer to paragraph 4.7 for a discussion of power considerations.

3. Set the 1260 POWER switch to the ON position. The red lamp in the center of the switch should be lighted.

4. Using a cord equipped with 310 plugs, insert one plug into the 1260 SEND/DROP jack and the other into the 1260 RCV/LINE jack.

5. Set the E&M/MON/LOOP switch to the LOOP position.

6. Set the BRIDGE/TERM switch to the TERM position.

7. Release all LOOP RES and LINE LEAK switches.

8. Set the ON HOOK/OFF HK-DIAL/CONT switch to the CONT position.

9. Set the RECEIVE and SEND mode switches to DRY LOOP.

10. Set the SPEED and % BREAK thumbwheel switches to some convenient combination such as 12 pps and 60 percent break. See Figure 4—2 for the graph defining the allowable combinations of pulse speed and percent break.

11. Depress the MAX and MIN pushbuttons simultaneously. The digital displays should be cleared and after a slight delay the speed and percent break set on the thumbwheel switches should appear on the digital display. Acceptable accuracy is ±0.1 pps and ±0.5 % break.

12. Depress and hold the MAX pushbutton. The display should agree with the values set on the thumbwheel for both the speed and percent break. Acceptable accuracy is ±0.1 pps and ±0.5 % break.

13. Depress and hold the MIN pushbutton. The display should agree with the values set on the thumbwheels for both speed and percent break. Acceptable accuracy is ±0.1 pps and ±0.5 % break.

14. Set the ON HOOK/OFF HK-DIAL/CONT switch to the OFF HK-DIAL position.

15. Depress the MAX and MIN pushbuttons simultaneously. The digital display should be cleared and remain cleared.

16. On the keypad, depress the 0 key. The digital display should agree with the values set in on the SPEED and % BREAK thumbwheels. Acceptable accuracy is ±0.1 pps and ±0.5 % break.

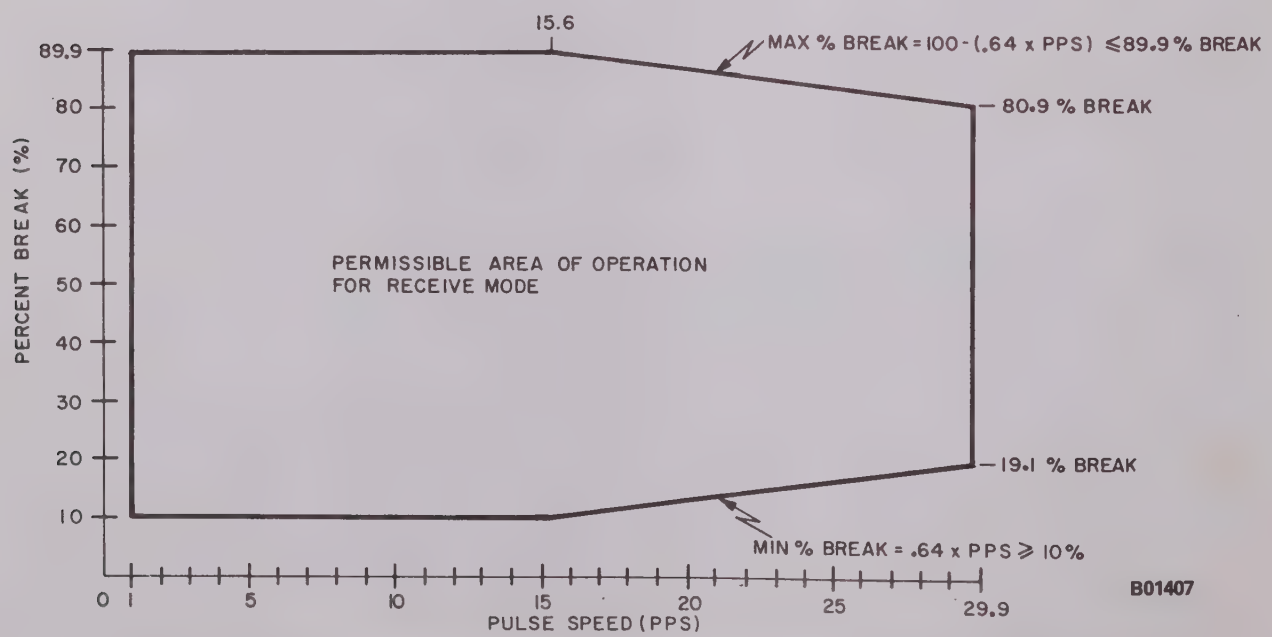


Figure 4—2. Receive Maximum And Minimum Percent Break Versus Pulse Speed

4.28 SENDING DRY OR WET LOOP

4.29 To send only on a dry or wet (battery and ground) basis, perform the following steps. See Figures 4—3 and 4—4 that show the relationships between the SEND jack and the internal circuits that define the conditions appearing at the tip and ring.

1. Insert a 310 plug into the 48V jack on the 1260 rear panel.

2. Connect the other end of the power cord to central office battery and ground. Refer to paragraph 4.7 for a discussion of power considerations.

3. Set the 1260 POWER switch to the ON position. The red lamp in the center of the switch should be lighted.

4. Set the 1260 E&M/MON/LOOP switch to the LOOP position.

5. Set the SEND mode switch to either the DRY LOOP or the WET LOOP position as required.

6. Set the ON HOOK/OFF HK-DIAL/CONT switch to the ON HOOK position.

7. Set the SPEED and % BREAK thumbwheel switches as required. Refer to paragraph 4.22 for pulsing speed and percent break considerations.

8. If required, depress the appropriate LOOP RES and LINE LEAK pushbuttons.

9. Insert a 310 plug into the SEND jack and connect the other end of the cord to the circuit to be pulsed.

10. To send a continuous stream of pulses, set the ON HOOK/OFF HK-DIAL/CONT switch to the CONT position.

11. To outpulse dialed digits using the keypad, set the ON HOOK/OFF HK-DIAL/CONT switch to the OFF HK-DIAL position and then depress the required keys. Refer to paragraph 4.9 for a discussion of the considerations when sending and receiving dialed pulses.

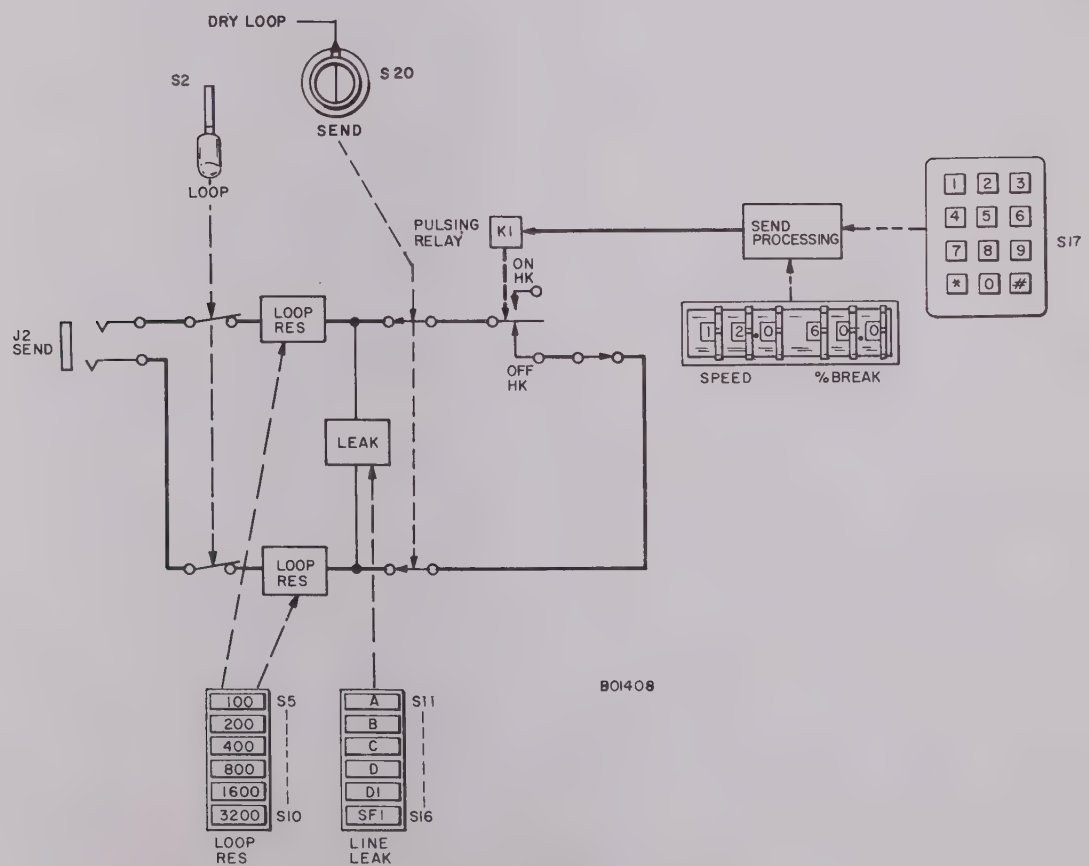
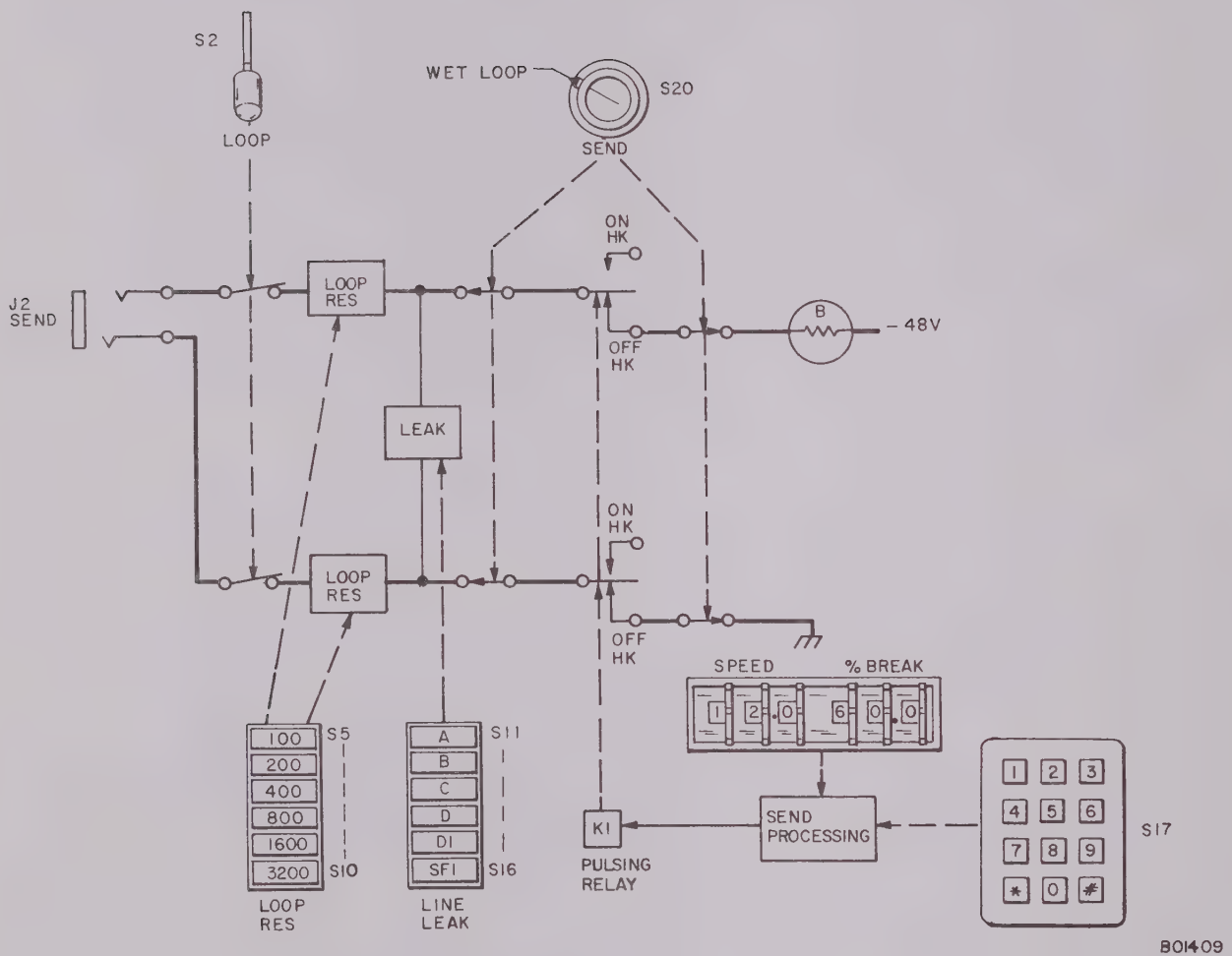


Figure 4—3. Sending Dry Loop



NOTES:
1. ⏚ = LOCAL OFFICE GROUND

Figure 4—4. Sending Wet Loop (Battery And Ground)

4.30 SENDING E&M

4.31 To send only either on the M lead toward the line or on the E lead toward the drop, perform the following steps. See Figure 4—5 for an illustration showing a typical interface between the Model 1260 and an E&M jackfield. Figures 4—6 and 4—7 illustrate the LINE and DROP jacks in relation to the internal circuits that define the conditions at the jacks.

1. Insert a 310 plug into the 48V jack on the 1260 rear panel.

2. Connect the other end of the power cord to central office battery and ground. Refer to paragraph 4.7 for a discussion of power considerations.

3. Set the 1260 POWER switch to the ON position. The red lamp in the center of the switch should be lighted.

4. Insert a dual 310 plug into the 1260 LINE and DROP jacks.

5. Insert the other end of the cord into the corresponding jacks of the E&M circuit to be pulsed.

6. Set the 1260 E&M/MON/LOOP switch to the MON position. The circuit being monitored is idle only when both monitor lamps are lighted.

7. Set the ON HOOK/OFF HK-DIAL/CONT switch to the ON HOOK position.

8. Set the E&M/MON/LOOP switch to the E&M position.

9. To send on the E lead toward the drop, set the SEND mode switch to either the E G&O or to the E G&B position as required.

10. To send on the M lead toward the line, set the SEND mode switch to either the M B&O or to the M B&G position as required.

11. When sending in the E and M modes, the 1260 jack in the reverse direction is automatically busied by the positioning of the SEND mode switch. Refer to paragraph 4.20 and to Table 4—3 for information on busy supervision.

12. Set the SPEED and % BREAK switches as required. Refer to paragraph 4.22 for pulse speed and percent break considerations.

13. For a continuous stream of pulses, set the ON HOOK/OFF HK-DIAL/CONT switch to the CONT position.

14. To outpulse dialed digits using the keypad, set the ON HOOK/OFF HK-DIAL/CONT switch to the OFF HK-DIAL position and then depress the required keys. Refer to paragraph 4.9 for a discussion of the considerations when sending and receiving dialed pulses.

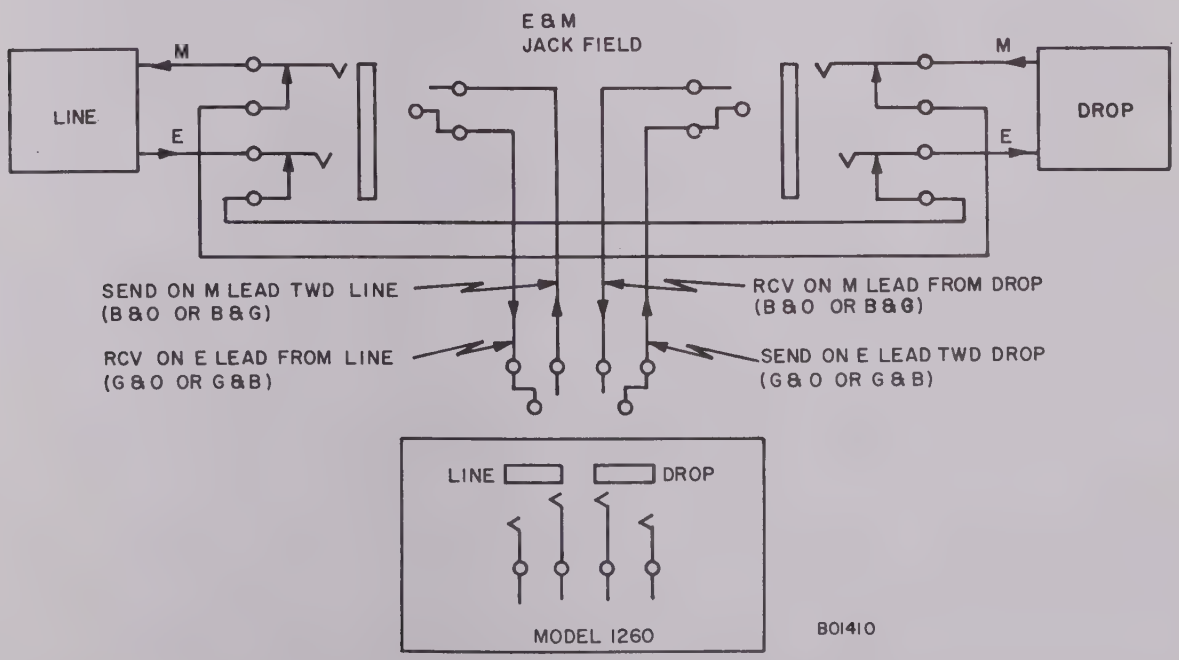


Figure 4—5. Typical Model 1260 Interface With E&M Circuits

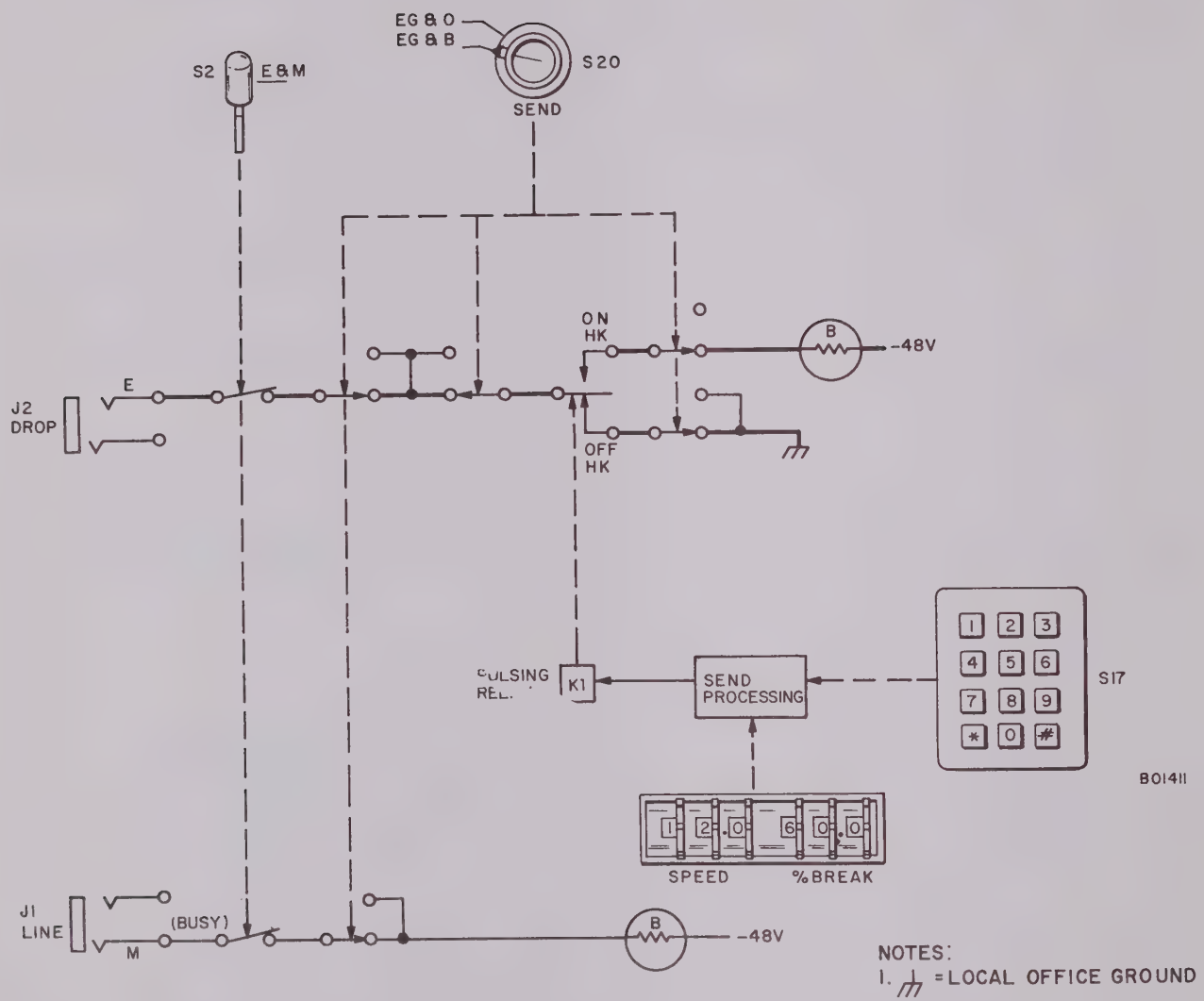


Figure 4—6. Sending On The E Lead Toward The Drop

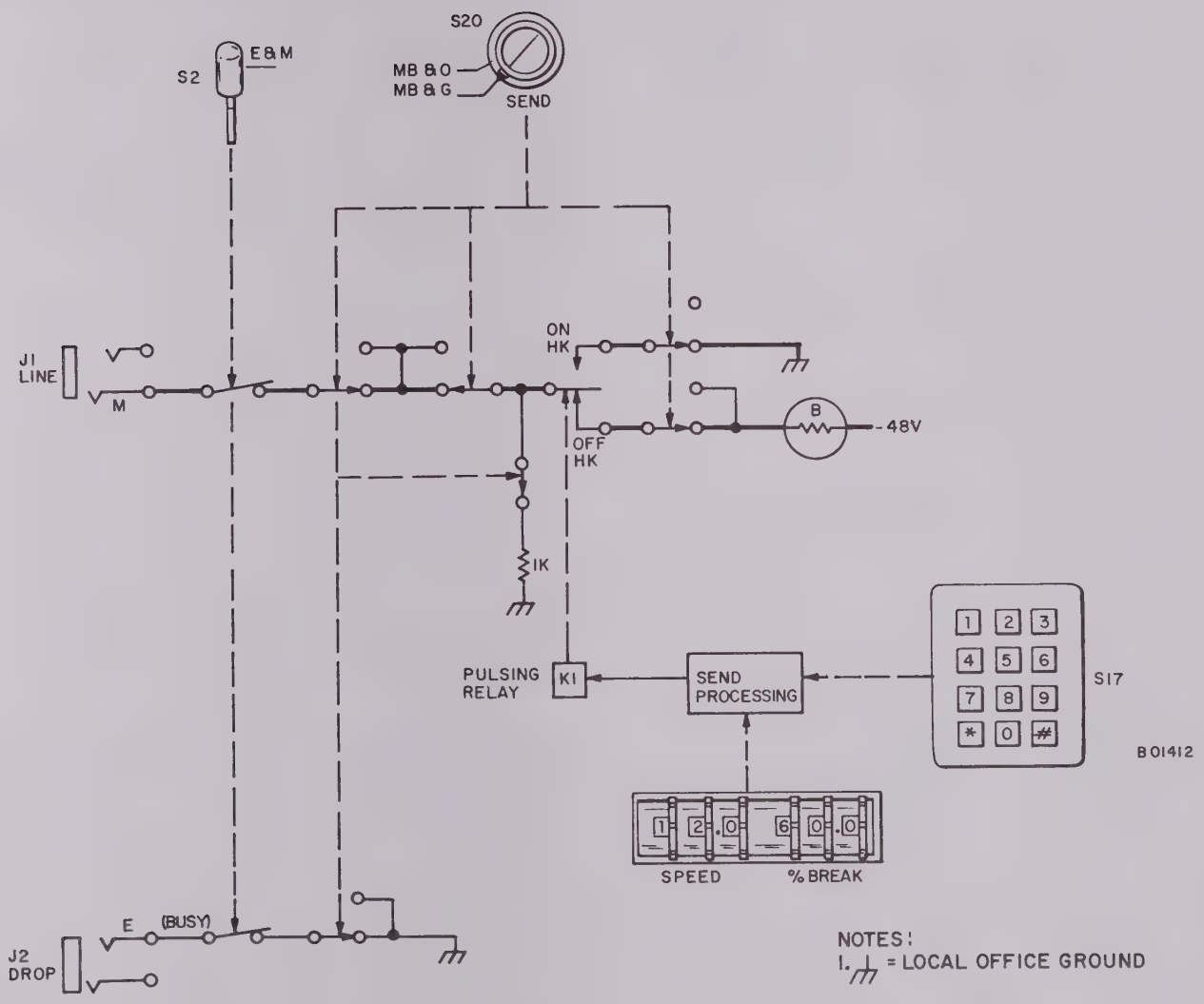


Figure 4—7. Sending On The M Lead Toward The Line

4.32 RECEIVING DRY OR WET LOOP

4.33 To receive only on a dry or wet loop (battery and ground) basis, perform the following steps. See Figures 4—8 and 4—9 for the illustrations that show the RCV jack in relation to the internal circuits that define the conditions at the tip and ring that can be measured.

NOTE

There are certain combinations of pulsing speed and percent break that the Model 1260 cannot measure. Refer to paragraph 4.22 and Figure 4—2 for information concerning this topic.

1. Insert a 310 plug into the 48V jack on the rear panel.

2. Connect the other end of the power cord to central office battery and ground. Refer to paragraph 4.7 for a discussion of power considerations.

3. Set the 1260 POWER switch to the ON position. The red lamp in the center of the switch should be lighted.

4. Insert a 310 plug into the 1260 RCV jack and connect the other end of the cord to the set of pulsing contacts to be measured.

NOTE

If a set of pulsing contacts is not conveniently available, use the "A" relay mounted on the 1260 rear panel. Connect the circuit to be measured to the COIL jack and the CONTACTS jack to the RCV jack on the front panel.

5. Set the 1260 E&M/MON/LOOP switch to the LOOP position.

6. To terminate the circuit under test in a low impedance, set the BRIDGE/TERM switch to the TERM position. If a high impedance is required, set the switch to the BRIDGE position.

7. Set the RECEIVE mode switch to either the DRY LOOP or the WET LOOP position as required.

8. Depress the MAX and MIN pushbuttons simultaneously. This will clear the digital display.

9. If receiving a continuous stream of pulses, the digital display will provide an indication of the average pulse speed and percent break after 10 pulses have been received and measured. The display will be updated automatically every 10 pulses measured thereafter.

10. When either the MAX or the MIN pushbutton is depressed separately, the display will indicate the maximum or minimum speed and percent break respectively that has been measured since the last time both pushbuttons were depressed simultaneously. When either of the pushbuttons is depressed, both the speed and percent break are displayed together. This does not imply that they necessarily occurred during the same pulse.

11. If desired, use the METER ADJ control to set the meter indication to agree with the digital indication. The meter can be used to observe short term pertubations in the received percent break. It also provides on-hook and off-hook indications.

12. If receiving and measuring dial-pulsed digits, refer to paragraph 4.9 for a discussion of the considerations that must be taken into account when sending and receiving dial-pulsed digits.

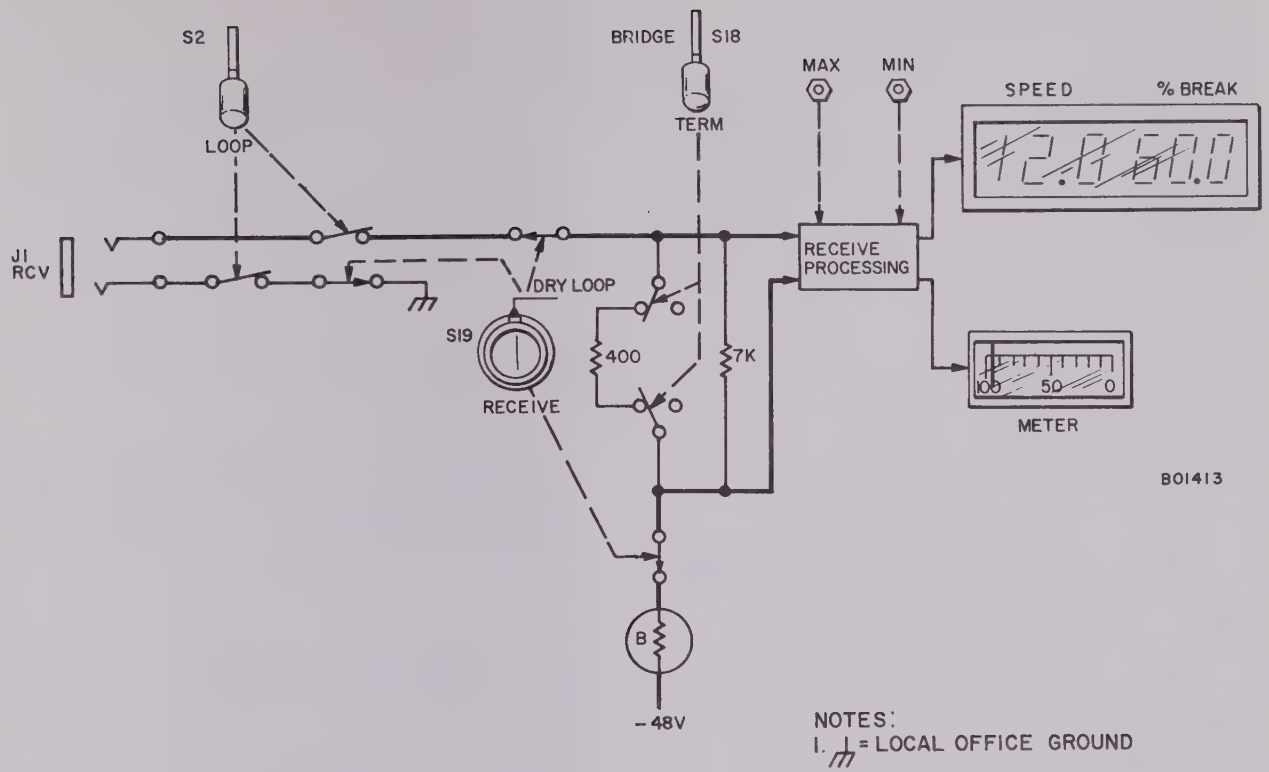
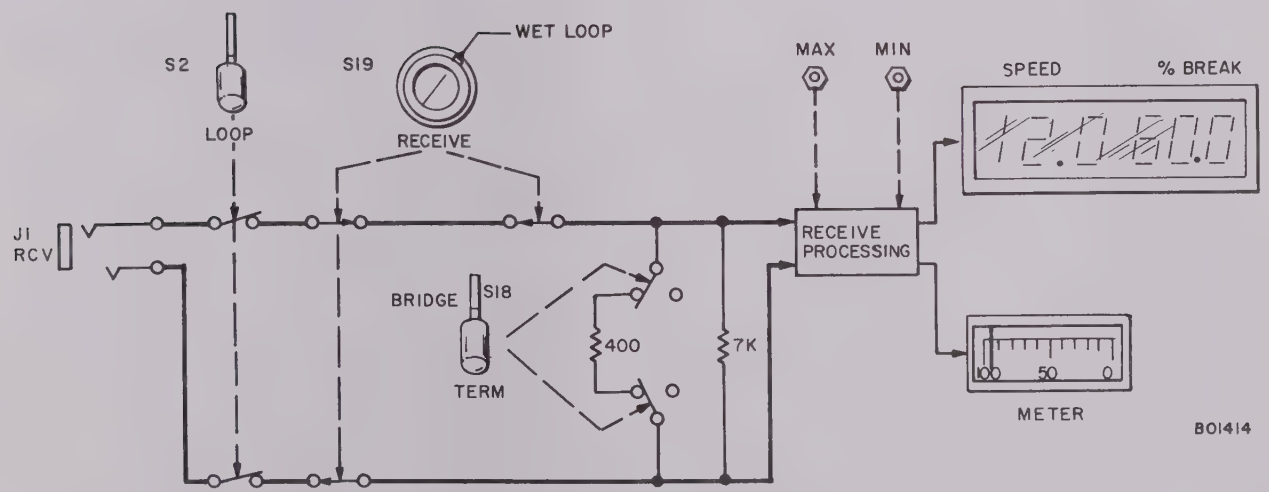


Figure 4—8. Receiving Dry Loop



NOTES:
1. J1 RING MUST BE PULSED G&O AND THE TIP B&O. IF THIS IS NOT THE CASE, REVERSE LEADS TO J1.

Figure 4—9. Receiving Wet Loop (Battery And Ground)

4.34 RECEIVING E&M

4.35 To receive only on the E lead from the line or on the M lead from the drop, perform the following steps. See Figure 4—5 for the illustration showing a typical interface between the Model 1260 and an E&M jackfield. See Figures 4—10 and 4—11 for the illustrations that show the relationship between the LINE and DROP jacks and the internal circuits that define the conditions at the jacks that can be measured.

1. Insert a 310 plug into the 48V jack on the 1260 rear panel.

2. Connect the other end of the power cord to the central office battery and ground. Refer to paragraph 4.7 for a discussion of power considerations.

3. Set the 1260 POWER switch to the ON position. The red lamp in the center of the switch should be lighted.

4. Set the 1260 E&M/MON/LOOP switch to the MON position.

5. Insert a dual 310 plug into the 1260 LINE and DROP jacks.

6. Insert the other end of the cord into the corresponding jacks at the E&M circuit to be measured.

7. The circuit is idle only when both monitor lamps on the 1260 are lighted.

8. Set the 1260 E&M/MON/LOOP switch to the E&M position.

9. To terminate the circuit under test in a low impedance, set the BRIDGE/TERM switch to the TERM position. For a high impedance, set the switch to the BRIDGE position.

10. Set the RECEIVE mode switch to either of the E positions or to either of the M positions as required.

11. To apply a reverse busy signal, the SEND mode switch must be set to the appropriate position. Refer to paragraph 4.20 and to Table 4—4 for information on this subject.

12. Depress the MAX and the MIN pushbuttons simultaneously. This will clear the digital display.

13. If receiving a continuous stream of pulses, the digital display will provide an indication of the average pulse speed and percent break after 10 pulses have been received and measured. The diplay will be updated automatically every 10 pulses measured thereafter.

14. When either the MAX or MIN pushbutton is depressed separately, the display will indicate the maximum or minimum speed and percent break respectively that has been measured since the last time both pushbuttons were depressed simultaneously. When either of the pushbuttons is depressed, both the speed and percent break are displayed together. This does not imply that they occurred during the same pulse.

15. If desired, use the METER ADJ control to set the meter indication to agree with the digital display. The meter can be used to observe short term pertubations in the received percent break. It also provides on-hook and off-hook indications.

16. If receiving and measuring dial-pulsed digits, refer to paragraph 4.9 for a discussion of the considerations that must be taken into account when sending and receiving dial-pulsed digits.

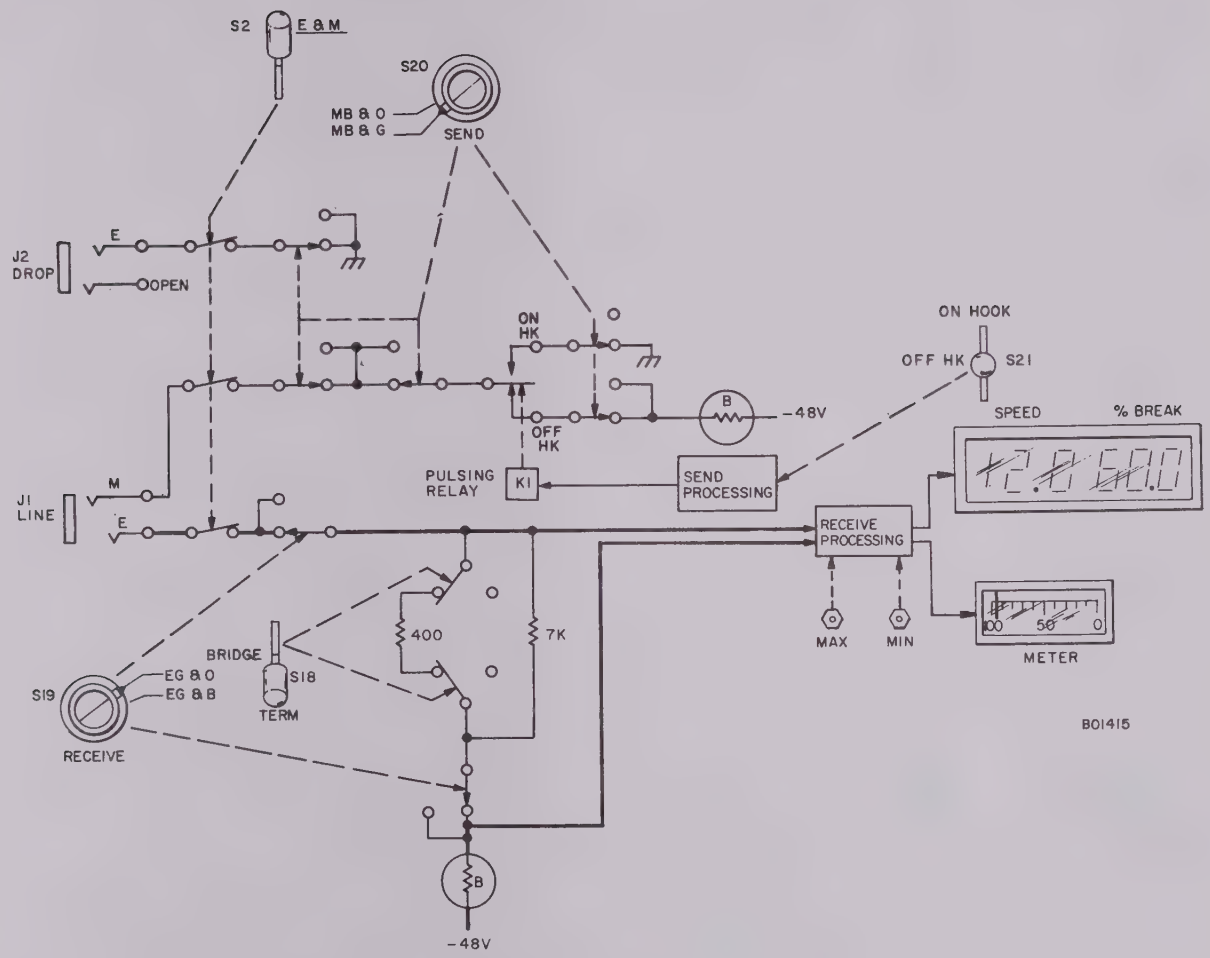


Figure 4—10. Receiving On The E Lead From The Line

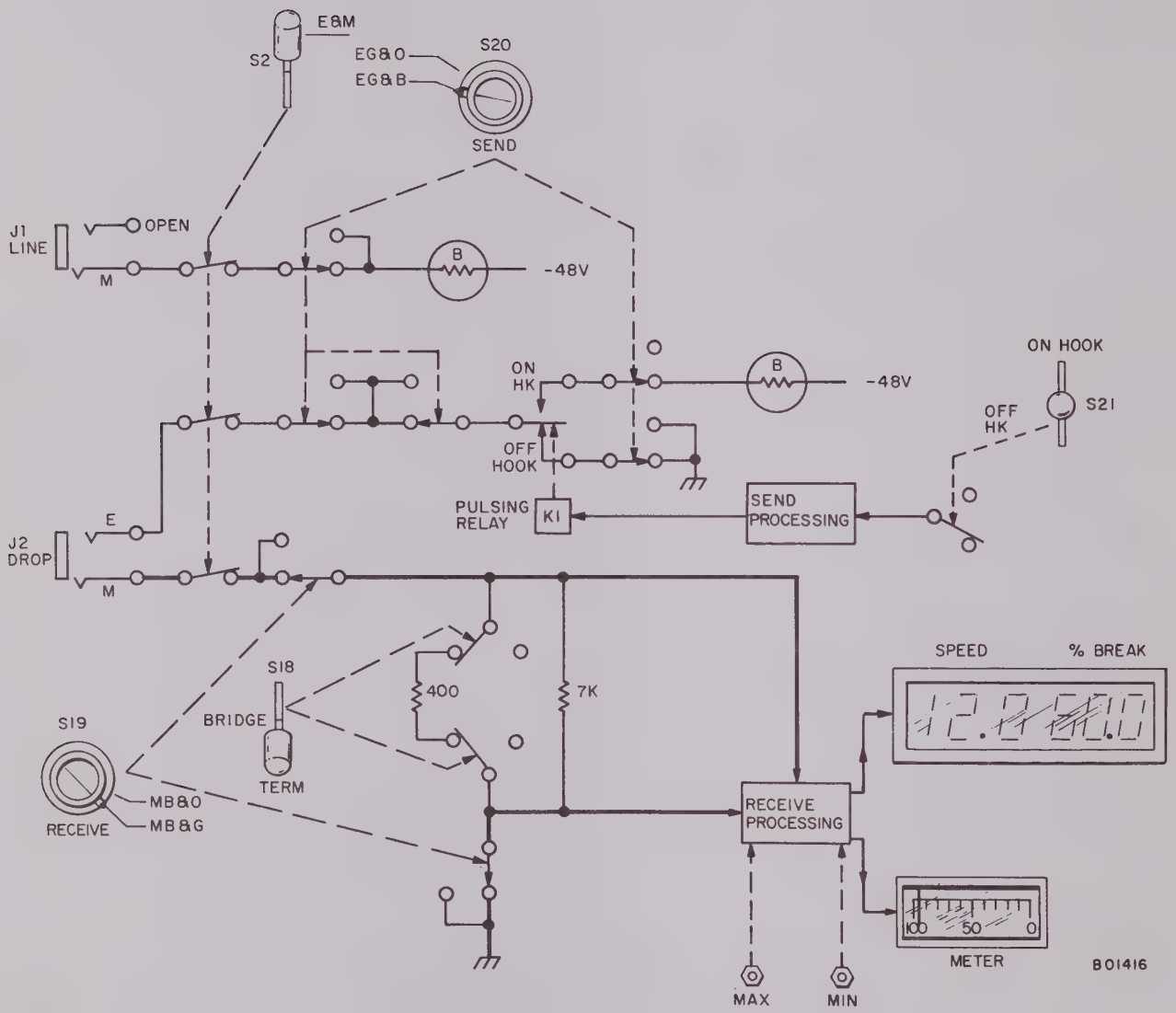


Figure 4—11. Receiving On The M Lead From The Drop

4.36 SENDING AND RECEIVING LOOP SIMULTANEOUSLY

4.37 When the circuit to be pulsed and the pulsing contacts to be measured are within a reasonable distance of each other, a single Model 1260 can be used to perform both functions simultaneously. The circuits to be pulsed and measured can also be totally independent. See Figures 4—3, 4—4, 4—8, and 4—9 for jack and internal circuit configurations for the send and receive loop modes. The dry and wet modes can be mixed in any of the four possible combinations of send and receive. Perform the following steps.

1. Insert a 310 plug into the 48V jack on the 1260 rear panel.

2. Connect the other end of the power cord to central office battery and ground. Refer to paragraph 4.7 for a discussion of power considerations.

3. Set the 1260 POWER switch to the ON position. The red lamp in the center of the switch should be lighted.

4. Set the 1260 E&M/MON/LOOP switch to the LOOP position.

5. Set the SEND mode switch to either the DRY LOOP or the WET LOOP position as required.

6. Set the ON HOOK/OFF HK-DIAL/CONT switch to the ON HOOK position.

7. Set the SPEED and % BREAK switches as required. Refer to paragraph 4.22 for a discussion of the permissible combinations of pulse speed and percent break.

8. If required, depress the appropriate LOOP RES and/or LINE LEAK pushbuttons.

9. To terminate the circuit under test in a low impedance, set the BRIDGE/TERM switch to the TERM position. For a high impedance, set it to the BRIDGE position.

10. Set the RECEIVE mode switch to either the DRY LOOP or the WET LOOP position as required.

11. Insert a 310 plug into the SEND jack and connect the other end of the cord to the circuit to be pulsed.

12. Insert a 310 plug into the RCV jack and connect the other end of the cord to the contacts to be measured.

NOTE

If a set of pulsing contacts is not conveniently available, use the "A" relay mounted on the 1260 rear panel. Connect the circuit to be measured to the COIL jack and connect the CONTACTS jack to the RCV jack on the front panel.

13. To send a continuous stream of pulses, set the ON HOOK/OFF HK-DIAL/CONT switch to the CONT positon.

14. To outpulse dialed digits using the keypad, set the ON HOOK/ OFF HK-DIAL/CONT switch to the OFF HK-DIAL position and then depress the required keys. Refer to paragraph 4.9 for a discussion of the considerations when sending and receiving dialed pulses.

15. Depress the MAX and MIN pushbuttons simultaneously. This will clear the display.

16. If using a continuous stream of pulses, the digital display will provide an indication of the average pulse speed and percent break after 10 pulses have been received and measured. The display will be updated automatically every 10 pulses measured thereafter.

17. When either the MAX or MIN pushbutton is depressed separately, the display will indicate the maximum or minimum speed and percent break respectively that has been measured since the last time both pushbuttons were depressed simultaneously. When either of the pushbuttons is depressed, both the speed and percent break are displayed together. This does not imply that they occurred during the same pulse.

18. If desired, use the METER ADJ control to set the meter indication to agree with the digital indication. The meter can be used to observe short term pertubations in the recieved percent break. It also provides on-hook and off-hook indications.

19. If using dialed digits, refer to paragraph 4.9 for a discussion of the important considerations.

4.38 SENDING AND RECEIVING E&M SIMULTANEOUSLY

4.39 When the circuit to be pulsed and the pulsing contacts to be measured are within a reasonable distance of each other, a single Model 1260 can be used to perform both functions simultaneously. The circuits to be pulsed and measured can also be totally independent. See Figures 4—5, 4—6, 4—7, 4—10, and 4—11 for the jack and internal circuit configurations for the send and receive E&M modes. The E and M modes can be mixed in any of the 16 possible combinations. Perform the following steps.

1. Insert a 310 plug into the 48V jack on the 1260 rear panel.

2. Connect the other end of the power cord to central office battery and ground. Refer to paragraph 4.7 for a discussion of power considerations.

3. Set the 1260 POWER switch to the ON position. The red lamp in the center of the switch should be lighted.

4. Set the 1260 E&M/MON/LOOP switch to the E&M position.

5. Set the SEND mode switch to any of the four E and M positions as required.

6. Set the RECEIVE mode switch to any of the four E and M positions as required.

7. To terminate the circuit under test in a low impedance, set the BRIDGE/TERM switch to the TERM position. For a high impedance, set the switch to the BRIDGE position.

8. Set the ON HOOK/OFF HK-DIAL/CONT switch to the ON HOOK position.

9. Set the SPEED and % BREAK switches as required. Refer to paragraph 4.22 for a discussion of the permissible combinations of pulse speed and percent break.

10. Insert a 310 plug into the 1260 SEND jack and connect the other end of the cord to the circuit to be pulsed.

11. Insert a 310 plug into the 1260 RCV jack and connect the other end of the cord to the pulsing contacts to be measured.

12. To send a continuous stream of pulses, set the ON HOOK/OFF HK-DIAL/CONT switch to the CONT position.

13. To outpulse dialed digits using the keypad, set the ON HOOK/OFF HK-DIAL/CONT switch to the OFF HK-DIAL position and then depress the required keys. Refer to paragraph 4.9 for a discussion of the important considerations when sending and receiving dialed pulses.

14. Depress the MAX and MIN pushbuttons simultaneously. This will clear the display.

15. If using a continuous stream of pulses, the digital display will provide an indication of the average pulse speed and percent break after 10 pulses have been received and measured. The display will be updated automatically every 10 pulses measured thereafter.

16. When either the MAX or MIN pushbutton is depressed separately, the display will indicate the maximum or minimum speed and percent break respectively that has been measured since the last time both pushbuttons were depressed simultaneously. When either of the pushbuttons is depressed, both the speed and percent break are displayed together. This does not imply that they occurred during the same pulse.

17. If desired, use the METER ADJ control to set the meter indication to agree with the digital indication. The meter can be used to observe short term pertubations in the received percent break. It also provides on-hook and off-hook indications.

18. If using dialed digits, refer to paragraph 4.9 for a discussion of the important considerations.

4.40 SENDING LOOP AND RECEIVING E&M, OR VICE VERSA

4.41 For checking such items as loop-to-E&M converters and E&M-to-loop converters, the Model 1260 provides a convenient mode of operation. All sending is done over the SEND jack and all receiving is through the RCV jack regardless of selected loop/E&M combinations. See Figures 4—12 through 4—15 for illustrations that show relationships between the jacks and internal circuits that define the conditions that can be sent and those that can be measured. To operate in mixed modes, perform the following steps.

1. Insert a 310 plug into the 48V jack on the 1260 rear panel.

2. Connect the other end of the power cord to central office battery and ground. Refer to paragraph 4.7 for a discussion of power considerations.

3. Set the 1260 POWER switch to the ON position. The red lamp in the center of the switch should be lighted.

4. Set the 1260 E&M/MON/LOOP switch to the LOOP position.

5. To **send loop and receive E&M,** set the SEND mode switch to either the DRY LOOP or WET LOOP position and the RECEIVE mode switch to any of the four E and M postions as required.

6. If sending loop, depress the appropriate LOOP RES and/or LINE LEAK pushbuttons as required.

7. To **send E&M and receive loop,** set the SEND mode switch to any of the four E&M positions and the RECEIVE mode switch to either the DRY LOOP or the WET LOOP position as required.

8. To terminate the circuit under test in a low impedance, set the BRIDGE/TERM switch to the TERM position. For a high impedance, set it to the BRIDGE position.

9. Set the ON HOOK/OFF HK-DIAL/CONT switch to the ON HOOK position.

10. Insert a 310 plug into the 1260 SEND jack and connect the other end to the circuit to be pulsed.

11. Insert a 310 plug into the 1260 RCV jack and connect the other end of the cord to the pulsing contacts to be measured.

12. To send a continuous stream of pulses, set the ON HOOK/OFF HK-DIAL/CONT switch to the CONT position.

13. To outpulse dialed digits using the keypad, set the ON HOOK/OFF HK-DIAL/CONT switch to the OFF HK-DIAL position and then depress the required keys. Refer to paragraph 4.9 for a discussion of the considerations when sending and receiving dialed pulses.

14. Depress the MAX and MIN pushbuttons simultaneously. This will clear the display.

15. If receiving a continuous stream of pulses, the digital display will provide an indication of the average pulse speed and percent break after 10 pulses have been received and measured. The display will be updated automatically every 10 pulses measured thereafter.

16. When either the MAX or MIN pushbutton is depressed separately, the display will indicate the maximum or minimum speed and percent break respectively that has been measured since the last time both pushbuttons were depressed simultaneously. When either of the pushbuttons is depressed, both the speed and percent break are displayed together. This does not imply that they occurred during the same pulse.

17. If desired, use the METER ADJ control to set the meter indication to agree with the digital display. The meter can be used to observe short term pertubations in the received percent break. It also provides on-hook and off-hook indications.

18. If using dialed digits, refer to paragraph 4.9 for a discussion of the important considerations.

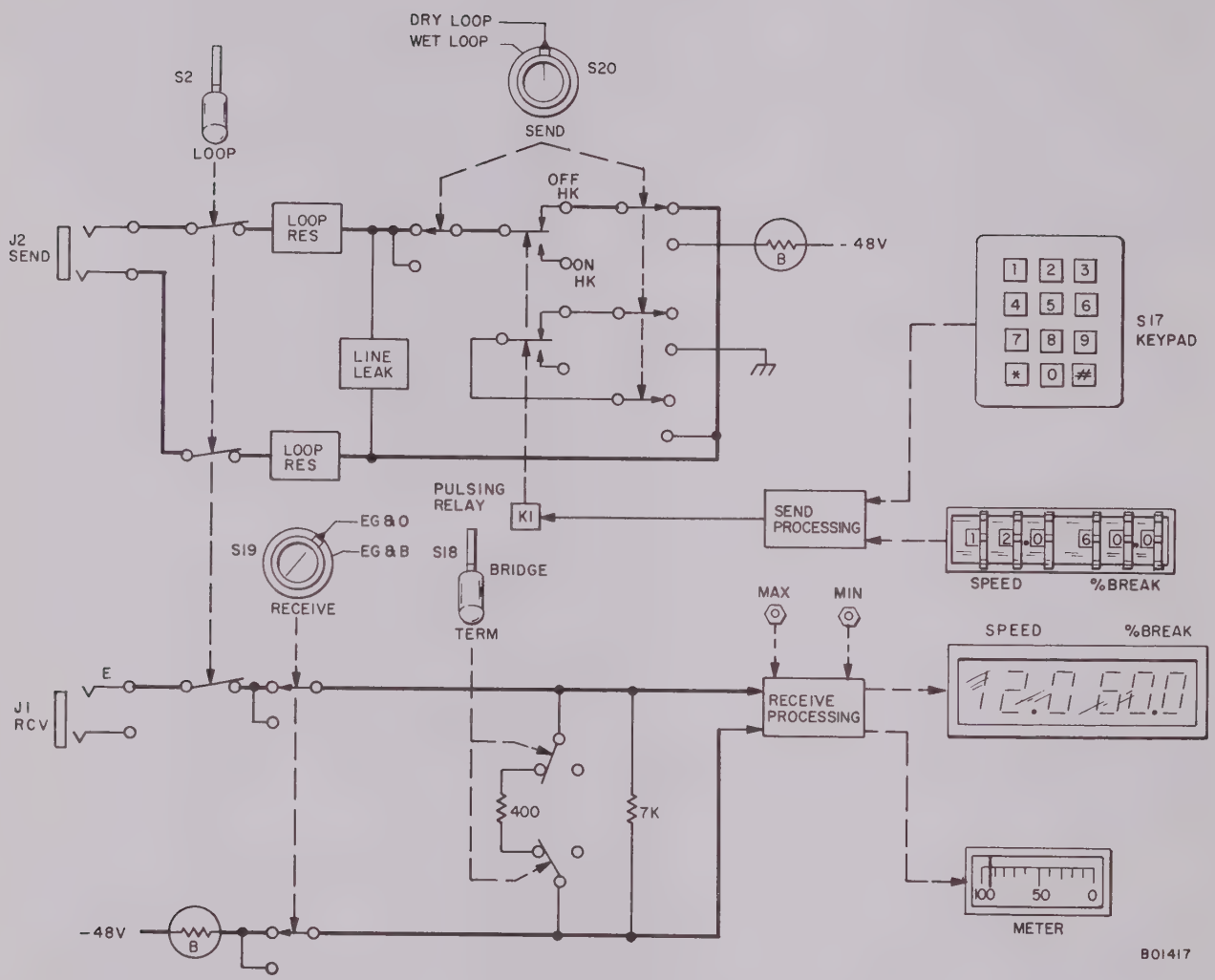


Figure 4—12. Sending Loop While Receiving On An E Lead

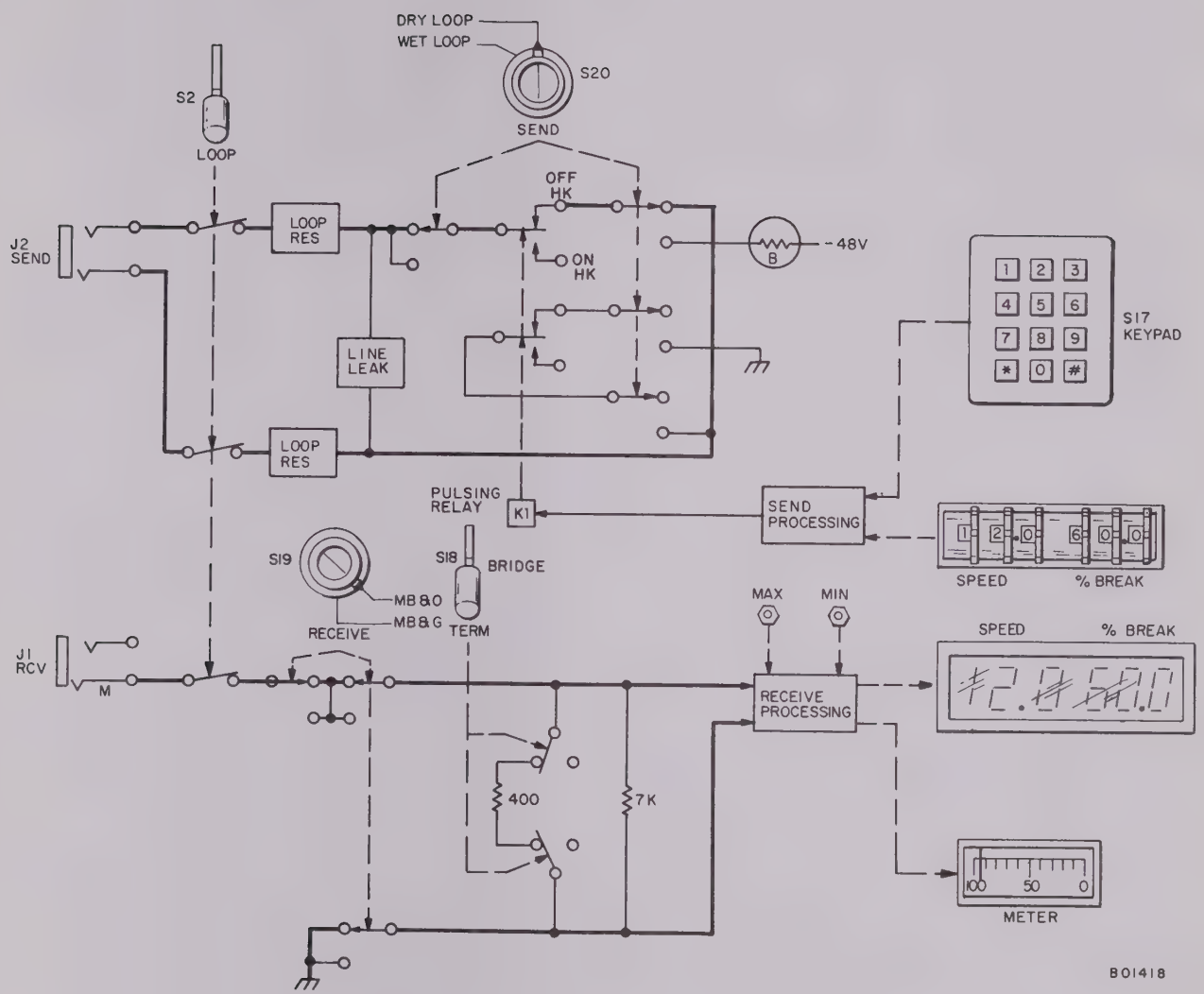


Figure 4—13. Sending Loop While Receiving On An M Lead

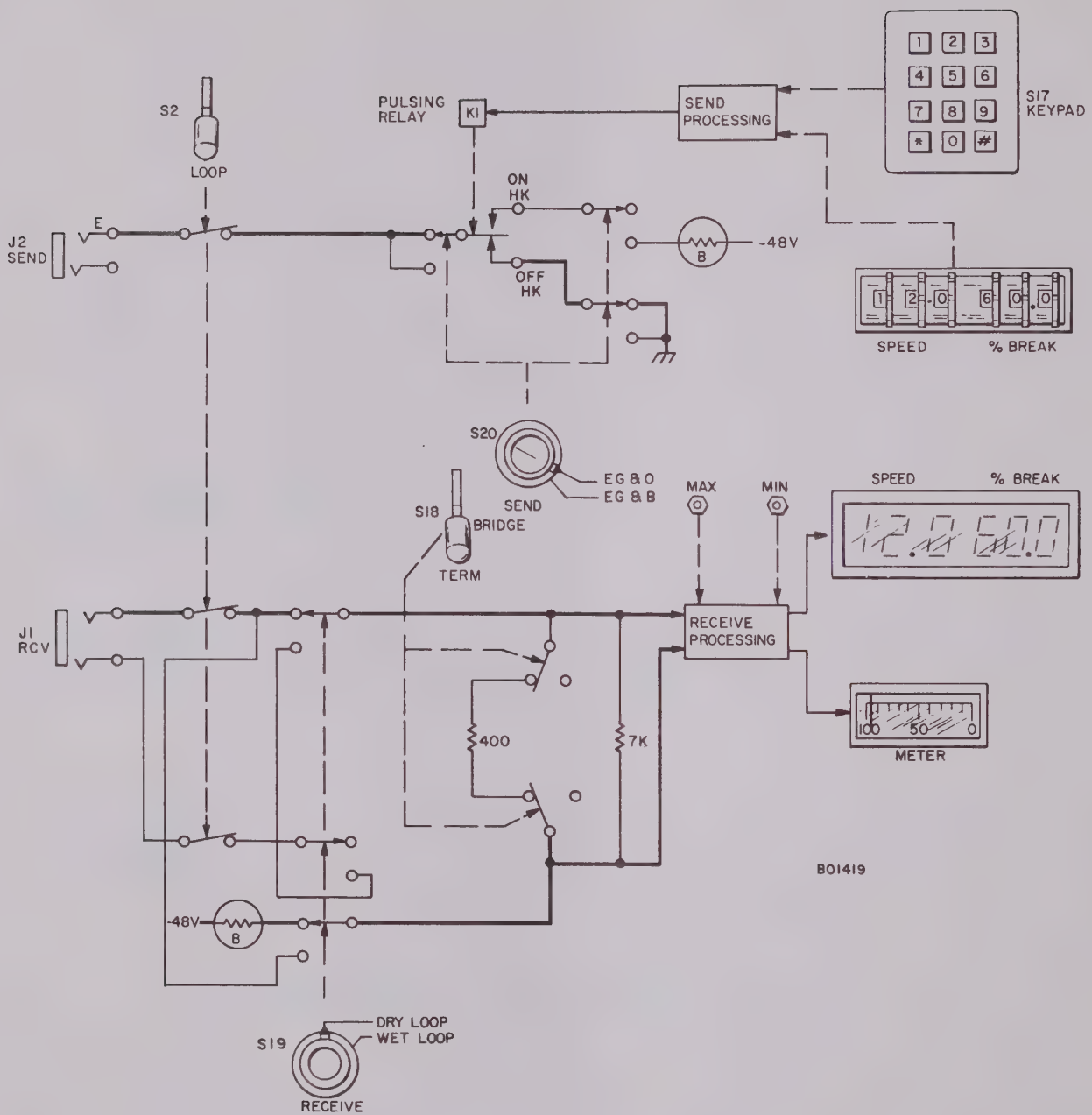


Figure 4—14. Sending On An E Lead While Receiving Loop

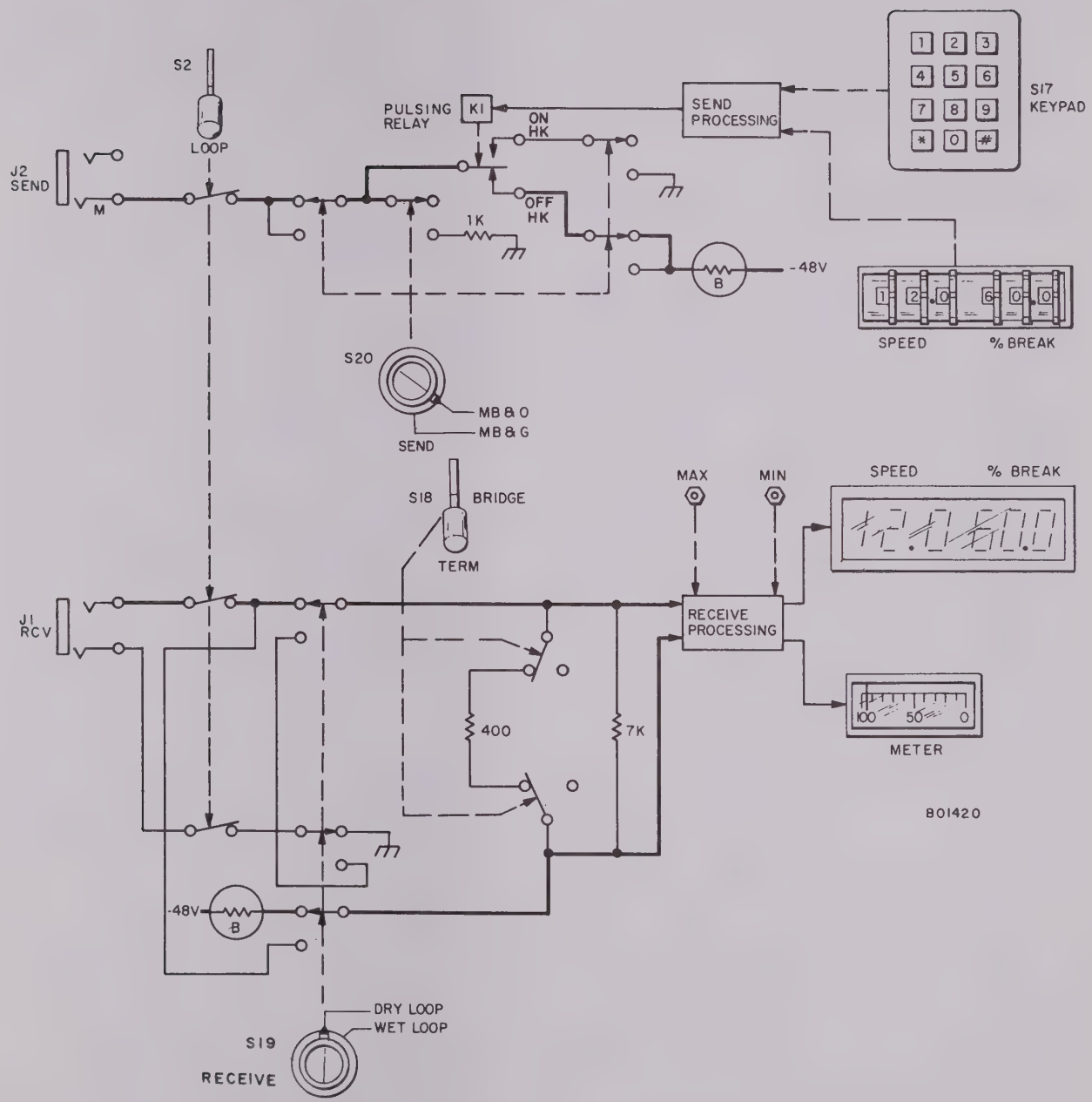


Figure 4—15. Sending On An M Lead While Receiving Loop

4.42 TESTING SPLIT COIL PULSING RELAYS

4.43 When testing a split coil pulsing relay, it may be difficult to disconnect the coil wires so that the 1260 can be used to pulse the relay. To use the 1260 to measure the pulsing speed and percent break of the driving relay contacts and the driven relay contacts without disconnecting any wires, perform the following steps.

1. Insert a 310 plug into the 48V jack on the 1260 rear panel.

2. Connect the other end of the 1260 power cord to central office battery and ground. Refer to paragraph 4.7 for a discussion of power considerations.

3. Set the 1260 POWER switch to the ON position. The red lamp in the center of the switch should be lighted.

4. Set the E&M/MON/LOOP switch to the LOOP position.

5. Set the BRIDGE/TERM switch to BRIDGE.

6. The driving relay pulsing can be measured either at point A or point B shown on Figure 4—16. If point A is used, connect point A to the ring of the RCV jack and set the RECEIVE mode switch to M B&G. If point B is used, connect point B to the tip of the RCV jack and set the RECEIVE mode switch to E G&B. The pulsing speed and percent break will be displayed.

7. Measure the driven contacts as instructed in paragraph 4.32.

4.44 USING THE 1260 AS A PRECISION LOOP DIALER WITH MONITOR FEATURE

4.45 When using the 1260 as a dialer, it may be desirable to employ a lineman's handset for monitoring and/or talking on the circuit under test. This is for two wire circuits only. To use a lineman's handset, perform the following steps.

1. Plug the circuit to be tested into the 1260's SEND jack.

2. Plug the lineman's handset into the 1260's RCV jack.

3. Set the E&M/MON/LOOP switch to LOOP.

4. Use the dial keypad on the 1260 to dial the desired number such as a milliwatt used to confirm the connection.

5. As soon as the connection is established, quickly set the E&M/MON/LOOP switch to MON. This connects the RCV and the SEND jacks in parallel so that the lineman's handset holds the circuit.

6. The handset can now be used for talking or monitoring on the circuit under test.

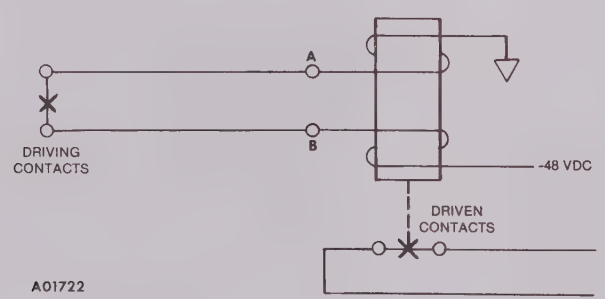


Figure 4—16. Testing Split Coil Relays

SECTION 5

THEORY OF OPERATION

5.1 This section provides the circuit descriptions for the Model 1260 Pulsing Test Set. Being a microcomputer-directed instrument, the 1260 is designed to have very definite functional sections. A detailed circuit description of each functional section is presented following an introductory overall block diagram description.

5.2 OVERALL BLOCK DIAGRAM DESCRIPTION

5.3 As shown on Figure 5—1, the Model 1260 is comprised of six functional sections: (1) the switch status function; (2) the dial keypad entry function; (3) the tranmitter function; (4) the monitor and reset function; (5) the receiver function and (6) the interrupt and display function. Except for the monitor part of the reset and monitor function, all of the other functional sections share the use of the processor, which consists of a CPU (central processing unit), a system controller, a clock generator, and memory.

5.4 All of the functional sections except the reset and monitor section operate on an I/O port basis. Data is transferred between the processor and the I/O ports over the data bus. Control of data transfer at the ports is a function of certain memory location addresses carried over the address bus as well as control lines applied to the control bus. Processor operation is under control of the stored program, or software, stored permanently in a portion of the memory.

5.5 The dial keypad entry function and part of the switch status function have indirect control over the transmitter section. The switch status function monitors the settings of the ON HOOK/OFF HK-DIAL/CONT switch and the SPEED and % BREAK thumbwheels to control these factors as they effect the transmitter section. The dial keypad entry function determines the digit to be transmitted when the ON HOOK/OFF HK-DIAL/CONT switch is in the DIAL position. The SEND mode switch, and the LOOP RES and LINE LEAK pushbuttons all effect the output line conditioning circuits of the transmitter function, and as such, are not under software control.

5.6 In the receiver functional section, the BRIDGE/TERM switch and the RECEIVE mode switch control the input interface circuits only and are not under software control. The meter simply monitors the received signal and displays the percent break plus on hook/off hook status. After the received signal has been taken control of by the processor, the interrupt and display section is continuously updated with the latest average pulsing speed and percent break data. A portion of the switch status function monitors requests for display of minimum and maximum speed and percent break data. When either the MIN or MAX pushbutton is pressed, the appropriate data is furnished by the processor and displayed.

5.7 The reset and monitor function performs the very important job of initializing operation of the processor each time the POWER switch is set to ON or whenever the E&M/MON/LOOP switch is set to (or passes through) the MON position. In addition, indicators show the status of the activity at the SEND and RCV jacks.

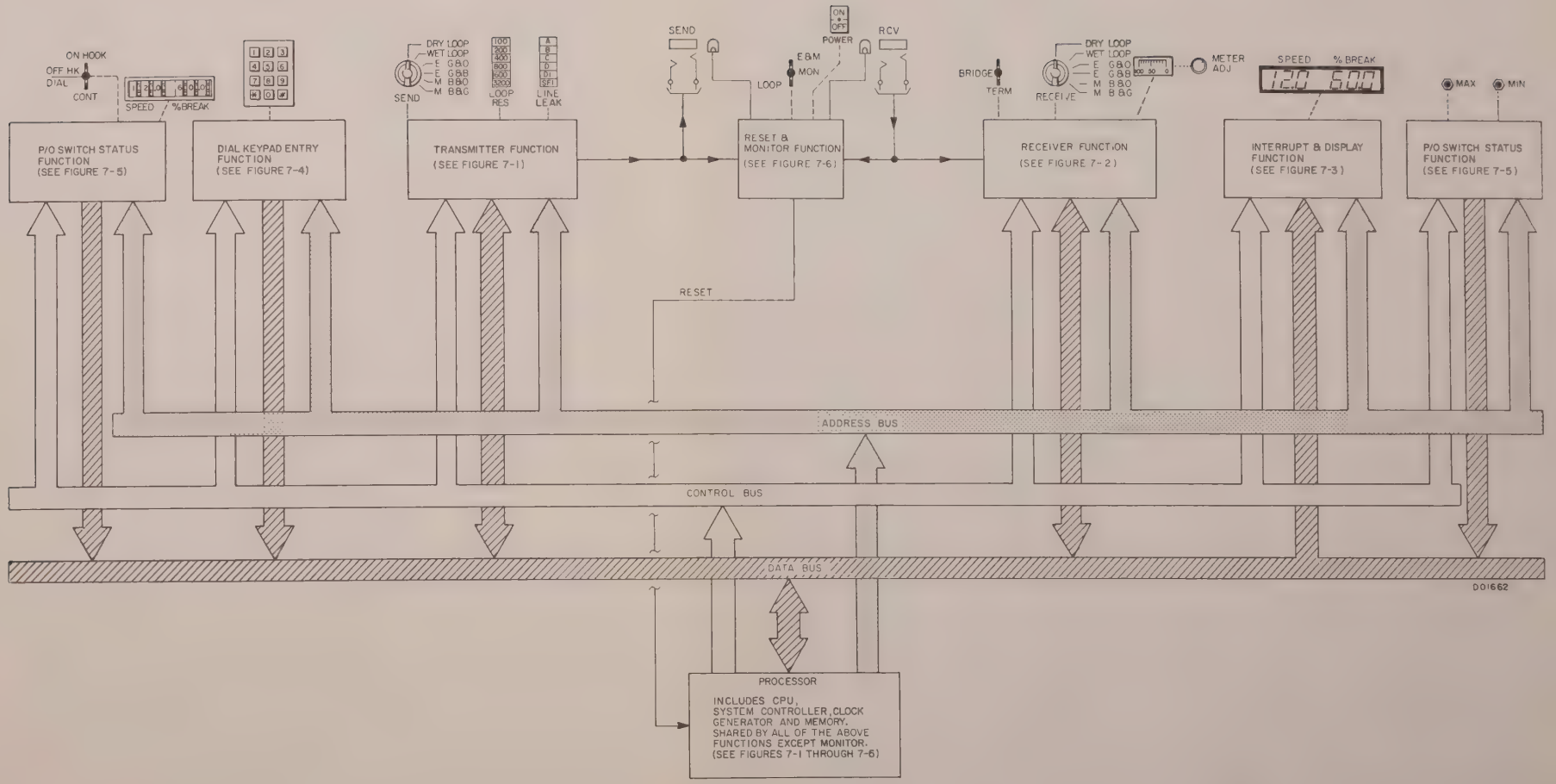


Figure 5—1. Model 1260 Overall Block Diagram

5.8 TRANSMITTER FUNCTION BLOCK DIAGRAM DESCRIPTION

5.9 Figure 5—2 shows a simplified block diagram of the transmitter function. The purpose of the transmitter is to generate break and make intervals that have the pulsing speed and percent break called for by the SEND controls. The processor converts the pulsing speed and percent break information it obtains from the front panel switches into digital words that are applied to the data bus. These words are then latched and later used to preset the counter. Decoded memory addresses control the movement of data within the transmitter. The number preset into the counter is the difference between the maximum count that the counter is capable of and the desired count. In this manner the number of pulses counted until the counter overflows, multiplied by the 25-microsecond period of the 40-kHz pulses counted, represents the desired time interval.

5.10 The resulting break and make intervals then represent the pulsing speed and percent break desired. The pulsing relay provides the interface between the transmitter circuits and the user. The type of pulsing at the SEND jack . . . such as dry loop, wet loop, or E&M . . . is a function of the line conditioning, which is set by the SEND mode switch. Line leak and loop resistance are added as required by front panel switches.

5.11 TRANSMITTER FUNCTION DETAILED CIRCUIT DESCRIPTION

5.12 See Figure 7—1 for the functional schematic diagram of the transmitter. The portion of the transmitter on the left hand page can be considered the digital section and that on the right hand page the analog section.

5.13 DIGITAL SECTION OF THE TRANSMITTER

5.14 The main function of the transmitter digital section is to generate break and make time intervals of the desired pulsing speed and percent break as set by the front panel switches and controlled by the software. This section consists of an address decoder, a 40-kHz generator, and a digital-to-time interval converter.

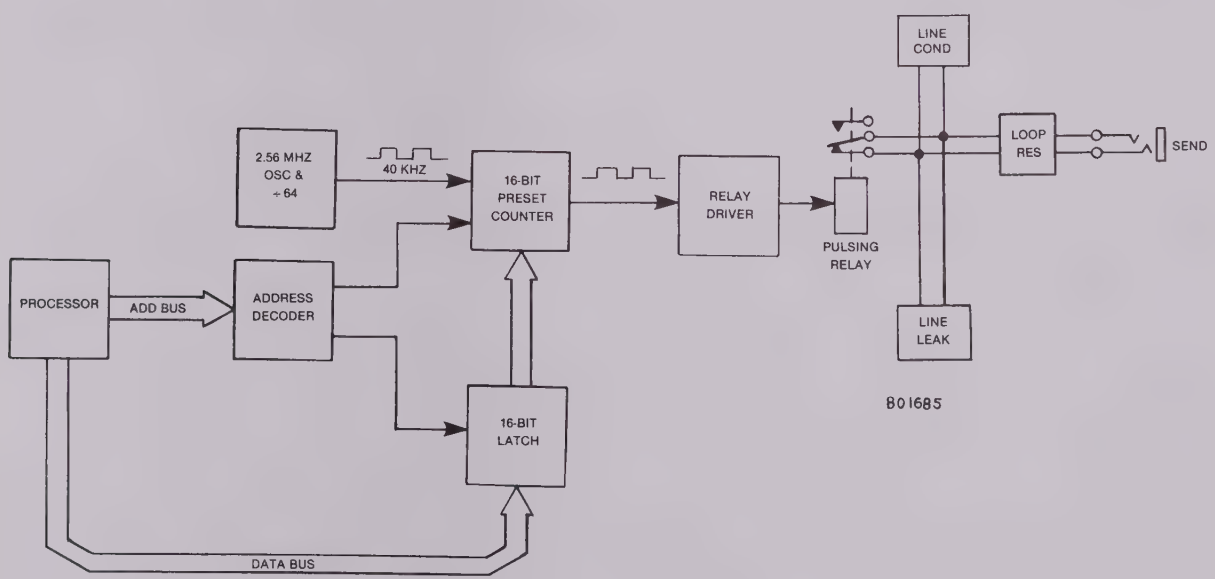


Figure 5—2. Transmitter Functional Section, Simplified Block Diagram

5.15 **Address Decoder**

5.16 The address decoder utilizes certain memory address locations placed on the address bus by the software to control the events occurring during the digital-to-time interval conversion. Address bits AØ through A4 and A8 through A15 in conjunction with control lines HLDA, $\overline{\text{MEMR}}$, and $\overline{\text{MEMW}}$ are used for address decoding. These are all outputs of CPU U9 and system controller U7 located on A8. The hold function of U9 is not used by the Model 1260 and, therefore, the HLDA output of U9 is always in the non-active or low state. This is used to permanently enable tri-state bus drivers U4, U5, and U6.

5.17 Address bits A8 through A15 are buffered by U5 and U6 and then applied to open collector AND gates U2A, U2B, and U2C. When A8 through A15 are all high the AND gate output goes high, is buffered by U4, and appears as an output line designated I/O. This corresponds to memory locations FFXXH and has been chosen to enable the I/O ports used in the 1260. The remaining five bits are buffered in U4 and U5 and are then designated ABØ through AB4. They form the XX parts of the general FFXXH locations. The final two lines used in decoding are $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ that are present at the output of U7 when there is a read or write command respectively.

5.18 Address decoders U16 and U17 located on A7 are devices that have two enable inputs and three binary inputs. When the G1 enable is high and the G2A/B enable is low, the Y outputs go low one at a time in accordance with the binary inputs. Tables 5—1 and 5—2 show how these inputs are decoded to form the 6 read and the 3 write command decodes.

5.19 **40-kHz Generator**

5.20 The technique of counting a known number of pulses to generate accurate time intervals by the digital-to-time interval converter requires a source of precision pulses. This is the function of the 40-kHz generator located on A6. U11 is a combination oscillator and divide-by-64 chip. Crystal Y1 allows a highly accurate 2.56-MHz signal to be generated by U11. After a division by 64, the 40-kHz output of U11 is applied to the 6 inverters of U10 connected in parallel. U11 is a CMOS device and U1D is TTL. The accumulative output drive capability of U10 is required to drive the input of U1D. Inverters U25B on A6 and U37B on A7 have Schmitt trigger inputs and generate the fast rise times required by the counting circuits that follow.

Table 5—1. Transmitter Read Address Decoding Truth Table

$\overline{\text{MEMR}}$	I/O	AB4	AB3	AB2	AB1	ABØ	FFØØH(R)	FFØ1H(R)	FFØ2H(R)	FFØ5H(R)	FFØ6H(R)	FFØ7H(R)
L	H	L	L	L	L	L	L	H	H	H	H	H
L	H	L	L	L	L	H	H	L	H	H	H	H
L	H	L	L	L	H	L	H	H	L	H	H	H
L	H	L	L	H	L	H	H	H	H	L	H	H
L	H	L	L	H	H	L	H	H	H	H	L	H
L	H	L	L	H	H	H	H	H	H	H	H	L

Table 5—2. Transmitter Write Address Decoding Truth Table

$\overline{\text{MEMW}}$	I/O	AB4	AB3	AB2	AB1	ABØ	FFØØH(W)	FFØ1H(W)	FFØ2H(W)
L	H	L	L	L	L	L	L	H	H
L	H	L	L	L	L	H	H	L	H
L	H	L	L	L	H	L	H	H	L

5.21 Digital-To-Time Interval Converter

5.22 The function of the digital-to-time converter is to generate the break and make time intervals from the 16-bit binary words supplied by the processor. Figure 5—3 is an event sequence diagram for the transmitter digital-to-time interval converter.

5.23 The basic technique used to generate precision time intervals is counting of the very accurate 40-kHz pulses (period of 25 microseconds). For example, the break interval for typical telephone signaling to be transmitted (10 pps pulsing speed at 50% break) is 50,000 microseconds. This would require counting 2,000 of the 40-kHz pulse periods.

5.24 One way this could be done would be to preset a counter to 2000, then count down to zero. However, the 1260 uses a counter that can count only in the up direction, so a different counter presetting technique must be used.

5.25 Returning to the example of counting 2000 of the 40-kHz pulses, the following presetting technique is used for the 1260's counter. The counter has a 16-bit length, thus a maximum count of 65,535. To count up 2000 counts to this number requires a decimal preset of 63,536. As a 16-bit binary word, this would be 1111 1000 0011 0000. This is a function of the processor. The counter will now count up 2000 counts until the counter overflows, at which time the counter will be in the all zeros state.

5.26 The sequence of events shown on Figure 5—3 represents the generation of a break interval followed by a make interval. It is assumed that the transmitter is in its idle condition such as it would be after power turn-on and initialization caused by the reset pulse. This clears U29B so that its Q output is low to inhibit the clock at U14A. Transmit flip-flop U18B is cleared and its Q output is placed off-hook (low).

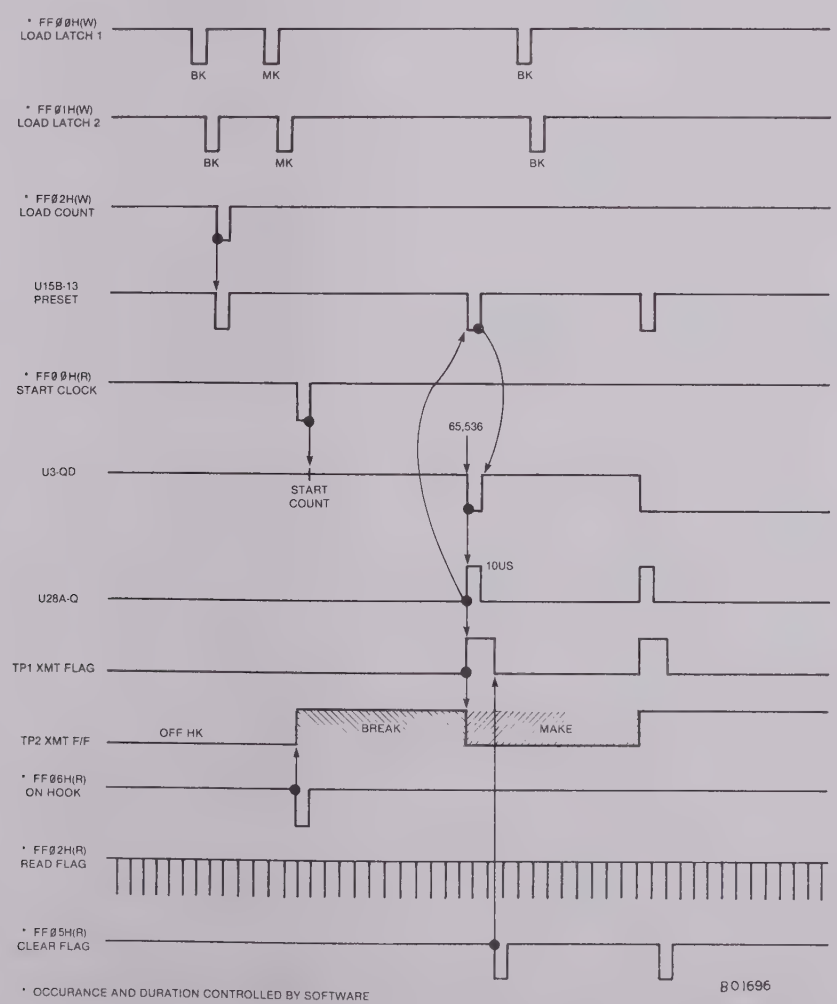


Figure 5—3. Event Sequence Diagram For The Transmitter Digital-To-Time Interval Conversion

5.27 The first interval generated is always a break interval. The sequence is started by decoding FFØØH(W) and FFØ1H(W) which latch the 16-bit break interval preset word into U11, U5, U8, and U2. This is immediately followed by FFØ2H(W) that is inverted by U13D and U15B and applied to the load input of all four preset counters. This presets the counters with the 16-bit break interval present at the output of the latches. Next FFØØH(W) and FFØ1H(W) are repeated to load the preset word for the following make interval into the latches. All of the required data for the first complete transmit pulse period has now been transferred from the processor to the digital-to-time interval converter; generation of the respective intervals is now ready to proceed.

5.28 Transmit enable address FFØØH(R) is decoded and presets U29B. The Q output enables U14A so that the 40-kHz pulses are applied to the counter. The counters now count up until 1 more than the maximum of 65,535 is reached, at which time the QD output of U3 goes low. This signals the end of the break interval. The 10-microsecond one-shot U28A is triggered by the negative QD transition and the U28A Q output is used to perform two tasks simultaneously.

1. It is applied through U15B to the load input of all counters to preset them with the make interval. (Note that, at the end of the 10-microsecond pulse, the counters again begin to totalize the make interval and the QD output of U3 goes high.

2. It clocks U18A to set the transmit flag high. The flag clocks U18B and the Q output of the transmit flip flop goes low to terminate the break interval. The flag is also applied to bus driver U1B.

5.29 The transmit flag is read onto the data bus by FFØ2H(R) to alert the processor that it must produce the next break preset data. The flag is immediately cleared by FFØ6H(R) and the count continues until the counter overflows, thus terminating the make interval. The process continues as long as a transmitter output is called for.

5.30 ANALOG SECTION OF THE TRANSMITTER

5.31 The transmitter signal at the input of inverter U24D consists of break and make intervals of the proper time duration. The break interval is high at this point and the make is low. During the break interval, Q4 conducts and turns on relay driver Q5. This allows pulsing relay K1 to energize and open its associated contacts. The schematic shown in Figure 7—1 depicts the unit in the dry loop mode so that the tip and ring of SEND jack J2 are opened during the break interval. Leak circuits located on A4 and loop resistance located on A3 are switched in as required. Switches S2 and S20 condition the actual pulsing contacts for dry loop, wet loop, and E&M signaling. See Figures 4—3, 4—4, 4—6, and 4—7 for the actual configurations.

5.32 RECEIVER FUNCTION BLOCK DIAGRAM DESCRIPTION

5.33 See Figure 5—4 for a simplified block diagram of the receiver. The function of the receiver is to convert the break and make time intervals present at the 1260's RCV jack into corresponding digital words that can be used by the processor in its computations of pulsing speed and percent break.

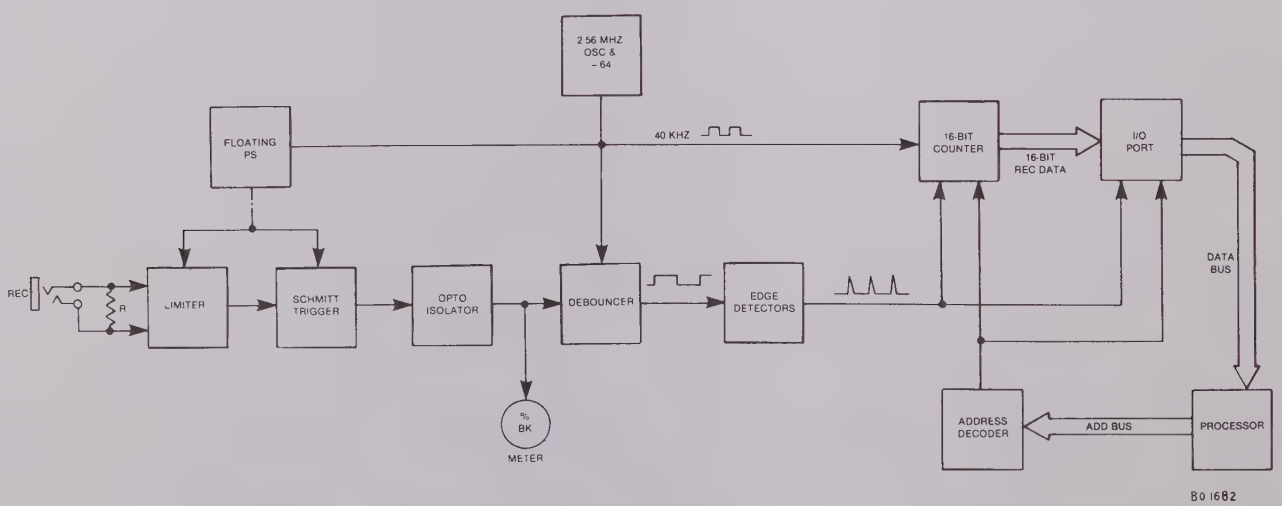


Figure 5—4. Receiver Functional Section, Simplified Block Diagram

5.34 The determination of whether a pulsing circuit connected to the RCV jack is in the make or break state is accomplished by sensing current through resistor R. The transition thresholds from make-to-break and vice versa are set by a limiter and a Schmitt trigger (which also squares-up the waveform). Both the limiter and Schmitt trigger are operated from a floating power supply. This isolates the circuits from office battery and ground and allows various combinations of battery, ground, and open to be applied across R. Further power supply isolation and level transformation is provided by an opto isolator. The output level of this stage is operated from +5 Vdc and is compatible with the TTL logic circuits that follow. The front panel % BK meter is driven by the opto isolator output.

5.35 Any contact bounce that may have been caused by the pulsing circuit generating the break and make intervals is still present at this point. A debouncer next removes all signal pertubations that occur within 6.4 milliseconds or less after the first transition. A 40-kHz waveform derived from the 2.56-MHz oscillator, provides the basic timing. At this point in the receiver, the break/make waveform has well defined edges and is now ready to be converted to an equivalent digital word.

5.36 The basic principle of the digital conversion technique used is to count 40-kHz pulses that occur during the time interval between edges of the waveform. Edge detectors provide well defined transitions that are used to gate the 16-bit counter on and off. Thus the break and make intervals are represented by 16-bit words that are proportional to the time intervals. Memory addresses furnished by the processor are decoded and used to control the transfer of the digital information from the counter to the I/O port and then to the processor itself.

5.37 RECEIVER FUNCTION DETAILED CIRCUIT DESCRIPTION

5.38 See Figure 7—2 for the functional schematic diagram of the receiver. The portion of the receiver shown on the left-hand page from RCV jack J1 to the output of the debounce circuit can be considered an analog circuit where the signal exists in the form of break and make time intervals. The remainder of the receiver shown on the right-hand page can be considered as the digital portion where the signal exists in the form of edges, pulses, and digital words.

5.39 ANALOG SECTION OF THE RECEIVER

5.40 The main function of this section is to detect break/make transitions and to generate a replica that has well-defined, debounced edges. Transition detection is done by sensing current through R4 located on A11. Current flows during the make interval, but not during the break interval. Regardless of the six combinations of battery, ground, and opens that can be received by the unit, S2 and S19 always connect R4 into the circuit such that when current does flow through the resistor, the top of R4 is positive with respect to the bottom. When the top of R4 is 9 volts or more positive than the bottom, the output of U21 goes high. Schmitt trigger U20 now rapidly switches, and its output goes high. Current now flows through the LED of opto isolator U19, and the light turns on the photo transistor. Thus an off hook (make) at the input to the 1260 is represented by a low level at TP6.

5.41 When the input goes from an off hook (make) to an on hook (break), current ceases to flow through R4. This means that there is no voltage drop across R4, and since U21 is connected in a voltage follower configuration, the U21 output is low. The input to the positive terminal of Schmitt trigger U20 is less than the reference voltage established by VR2, and the output of U20 rapidly switches to a low level, the opto isolator is cut off, and the voltage at TP6 is pulled high through R77.

5.42 Both U21 and U20 are operated from a floating power supply. The power supply is comprised of U13B, U12, T1, and diode rectifiers CR1, CR2, CR4, and CR5. The input to U13B is a 40-kHz squarewave. Complementary outputs of U13B are applied to the two inputs of driver U12. Transients at the outputs are limited to 12 volts by diodes CR6 and CR3. Transformer T1 generates a voltage waveform at its secondary. This is rectified by the bridge rectifier and filtered by C20 to produce +VI that is approximately 12 Vdc. The input to limiter U21 is also diode clamped to this level.

5.43 The rise times of the opto isolator output are not fast enough for the TTL logic that follows and, therefore, must be sharpened. Inverters U25C and U25D have Schmitt trigger inputs and produce outputs with greatly decreased rise times. After two more inversions in U22B and U1E, the opto isolator output is applied to % BK meter M1. An off hook causes the meter to deflect full scale and indicates OFF HK. On the other hand, an on hook input causes no current in the meter and it indicates ON HK.

5.44 The conversion technique used by the 1260 to create digital words proportional to received break and make intervals requires a source that has a frequency of high precision. U11 is an oscillator and a divide-by-64 circuit that produces a 40-kHz squarewave output. Crystal Y1 operates at 2.56 MHz and determines the basic operating frequency. Inverters U10A through U10F and U1D sharpen the rise times and furnish the required drive current. The 40-kHz squarewave is used

both by the debounce circuit and by the time interval-to-digital converter.

5.45 A decision of major importance that must be made by the 1260 is to determine when the input has gone from on hook (break) to off hook (make) and vice versa. The transitions are almost never clean; they are typically accompanied by several cycles of contact bounce. The function of the debounce circuit is to remove the normal contact bounce and generate a replica of the break and make intervals that has well-defined edges.

5.46 See Figure 5—5 for a typical timing diagram of the debounce circuit. One break and one make interval (with contact bounce) are shown. This requires the regeneration of three edges. As a starting point, it is assumed that flip flops U14A and U13A are cleared and that the input to U14A-CK is in a steady make (off hook) state. The first break-to-make transition of the input sets U14A and causes its Q output to go high. It should be noted that the 1260 always interprets the first transition, whether it is followed by contact bounce or not, as the legitimate start of the 6.4-millisecond debounce interval.

5.47 The input to U14A is inverted by U22B and becomes the clock input to U13A. This arrangement assures that every edge (including contact bounce) of the input signal is registered. The first contact bounce transition is used to clock U13A and the U13A output goes high. This is applied through U22C and clears U14A. The U14A Q output goes low. The high Q output of U13A is now applied through U22A and U24A to keep U24B enabled and the 6.4-millisecond debounce period continues.

5.48 The next contact bounce transition sets U14A's output high. This clears U13A through U22D, and also keeps U24B enabled. After counting 256 pulses (6.4 milliseconds) the 2QD output of counter U23 goes low. This is inverted by U24C and clocks flip flop U14B to trigger 5-microsecond one-shot U15A. If the input is still high, i.e., all contact bounce is completed, U14B will be set and its Q output will go high. The 5-microsecond pulse generated at the Q output of U15A is used to clear U14A.

5.49 The circuit is now again in a steady state and awaiting the first on hook-to-off hook transition. This transition will be registered by U13A and start the 6.4-millisecond debounce period as just described. At the end of the debounce period, and if the input is still low, U14B will be cleared to a low Q output.

5.50 The result of the debounce circuit is thus to generate, at the Q output of U14B, a replica of the input present at the CK input of U14A delayed by 6.4 milliseconds and with all contact bounce removed. If contact bounce lasts longer than 6.4 milliseconds, the output of U14B is unpredictable. The Q output of U14B is buffered by U25A before application to the digital section of the receiver.

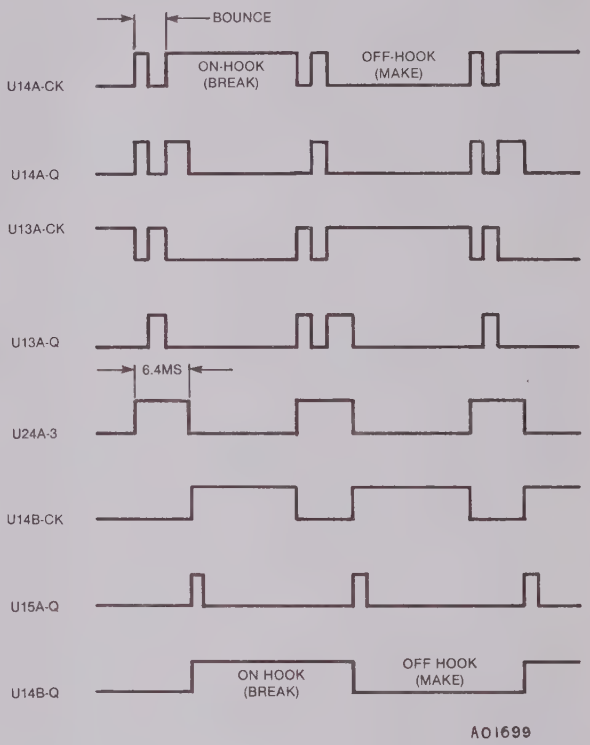


Figure 5—5. Timing Diagram For The Receiver Debounce Circuit

5.51 DIGITAL SECTION OF THE RECEIVER

5.52 The digital section of the receiver is comprised of an address decoder, edge detectors, and a time interval-to-digital converter. These circuits are shown on the right-hand page of Figure 7—2.

5.53 Address Decoder

5.54 The address decoding utilizes certain memory address locations placed on the address bus by the software to control the events occurring during the time interval-to-digital conversion. Address bits AØ through A4 and A8 through A15, in conjunction with control lines HLDA and $\overline{\text{MEMR}}$ are used for address decoding. These are all outputs of CPU U9 and system controller U7 located on A8. The hold function of U9 is not used by the 1260 and, therefore, the HLDA output of U9 is always in the non-active or low state. This is used to permanently enable tri-state bus drivers U4, U5, and U6.

5.55 Address bits A8 through A15 are buffered by U5 and U6 and then applied to open collector AND gates U2A, U2B, and U2C. When A8 through A15 are all high, the AND gate output goes high, is buffered in U4, and appears as an output line designated I/O This corresponds to memory locations FFXXH and has been chosen to enable the I/O ports used in the 1260. The remaining five bits are buffered in U4 and U5 and are then designated ABØ through AB4. They form the XX parts of the general FFXXH locations. The final line used in decoding is $\overline{\text{MEMR}}$ that is present at the output of U7 anytime there is a read command.

5.56 Address decoder U33 located on A7 is a device that has two enable inputs and three binary inputs. When the G1 enable is high and the G2A/B enable is low, the Y outputs go low one at a time in accordance with the binary input code. Table 5—3 shows how these inputs are decoded to form FFØ8H(R), FFØ9H(R), FFØAH(R), FFØBH(R), FFØCH(R), and FFØDH(R).

5.57 Edge Detectors And Time Interval-To-Digital Converter

5.58 The edge detectors and time interval-to-digital converter generates 16-bit binary words that represent the break and make time intervals. These words are then used by the processor to compute the pulsing speed and percent break and to ultimately display the results.

5.59 The 40-kHz pulses from A6 are inverted by U37B and applied to U36A. The debounced analog receive signal is inverted by U37A and applied to U36B. At the time a reset pulse is generated at power on, FFØAH(R) goes low to preset U32B. This sets the Q output high to enable both U36A and U36B for all normal operating modes. Thus the 40-kHz pulses and the analog signal are applied to the counters and edge detector all of the time.

5.60 See Figure 5—6 for the event sequence diagram that represents the time interval-to-digital conversion function. This converstion process can be represented by considering what happens to an on hook (break) interval followed by an off hook (make) interval. On the diagram these are represented by t_1 and t_2, which are defined by edges E1, E2, and E3.

5.61 Edge detectors U34B and U34A are 5-microsecond one-shots. Each negative edge of the analog signal triggers U34A, which produces a negative pulse at its Q output. Each positive edge, on the other hand, triggers U34B. When the outputs of these two one-shots are applied to OR gate U36D, the OR gate has one positive pulse for each edge of the analog signal.

5.62 These positive pulses are used to trigger one-shot U30A and strobe the counter data into the I/O ports. The 5-microsecond positive pulse present at the Q output of U30A is used to clear the counters to zero and to set flag flip flop U29A. The result so far in the process of converting t_1 to a digital word is as follows:

1. Edge E1 has been detected;

2. Then, 5 microseconds later, the counters are cleared to zero so that they immediately begin to totalize 40-kHz pulses for the measurement of t_1;

3. The receive flag, as present at TP3, is set high to alert the processor to the fact that an edge has occurred.

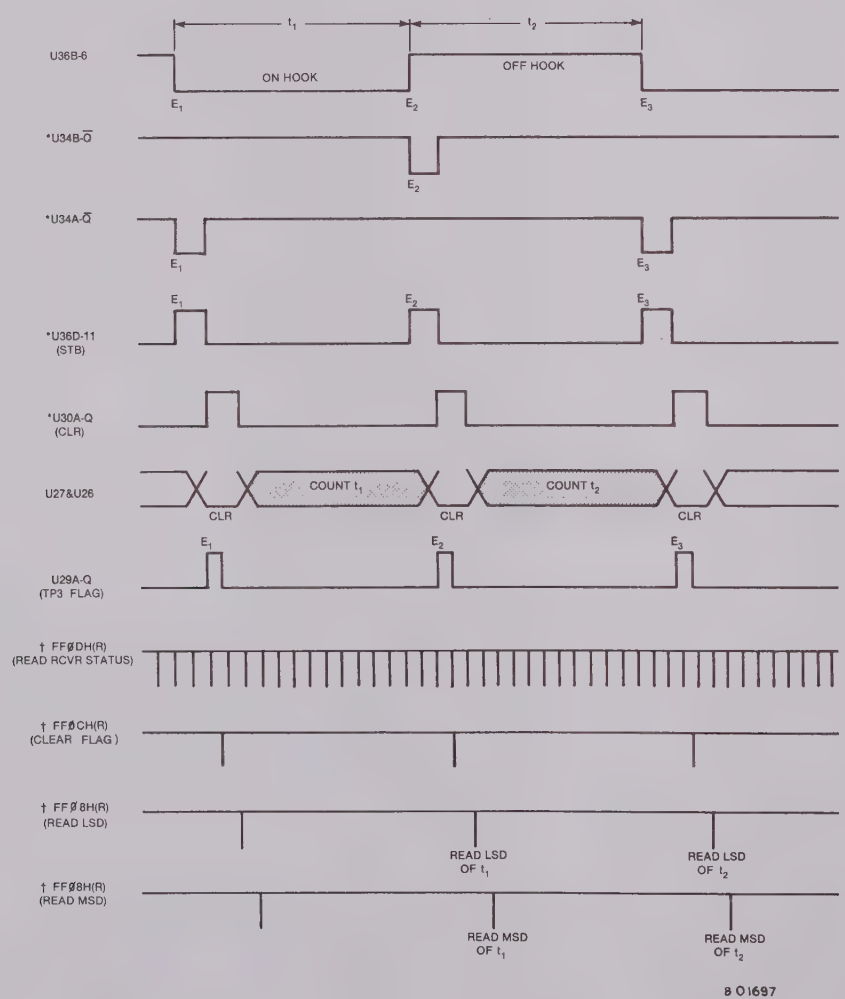
5.63 Approximately once each millisecond, the interrupt service routine causes FFØDH(R) to go low. This enables tri-state bus drivers in U25 and the receive flag, and the state of the analog signal at that instant is placed onto the data bus for application to the processor. The presence of the flag causes the software to assume temporary control of the digital receiver operation. The level of the analog signal just after the edge was detected is called the tip-ring status and is used by the processor to determine if the previous interval just measured was break or make. Very soon, FFØCH(R) goes low to clear the flag flip flop in anticipation of detecting edge E2.

5.64 The detection of E2 signals the end of t_1 and the following events occur. The positive pulse at the output of U36D strobes the t_1 count accumulated by U27 and U26 into I/O ports U24 and U23. The data does not appear on the bus as yet. Five microseconds later the counters are cleared to zero and start to totalize the count for t_2. Also the flag is again set at this time. After FFØDH(R) and FFØCH(R) read and clear the flag respectively, the data representing t_1 is now ready to be placed on the data bus. In rapid succession FFØ8H(R) and FFØ9F(R) go low and read the eight least significant bits and the eight most significant bits onto the bus.

5.65 The t_2 data count is next terminated with the detection of edge E3. Operation is as previously described, and the digital word is placed on the bus. All data on the bus is buffered by system controller U7 located on A8. The buffered data is then applied to the CPU for use in computations.

Table 5—3. Receiver Address Decoding Truth Table

$\overline{MEMR}$	I/O	AB4	AB3	AB2	AB1	ABØ	FFØ8H(R)	FFØ9H(R)	FFØAH(R)	FFØBH(R)	FFØCH(R)	FFØDH(R)
L	H	L	H	L	L	L	L	H	H	H	H	H
L	H	L	H	L	L	H	H	L	H	H	H	H
L	H	L	H	L	H	L	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H
L	H	L	H	H	L	L	H	H	H	H	L	H
L	H	L	H	H	L	H	H	H	H	H	H	L



* 5US PULSES NOT SHOWN TO SCALE.
† OCCURANCE AND DURATION CONTROLLED BY SOFTWARE

Figure 5—6. Event Sequence Diagram For The Receiver Time Interval-To-Digital Conversion

5.66 INTERRUPT AND DISPLAY FUNCTION BLOCK DIAGRAM DESCRIPTION

5.67 See Figure 5—7 for a simplified block diagram of the interrupt and display functional section. The purpose of the section is to continuously generate a repetitive interrupt signal and to display the pulsing speed and percent break data.

5.68 Addresses supplied by the processor are decoded and used to trigger an interrupt one-shot and to latch display data. Four of the latched bits are decoded and used to drive the seven-segment displays. Three more bits are decoded and used to multiplex the data among the six digits of the display.

5.69 INTERRUPT AND DISPLAY FUNCTION DETAILED CIRCUIT DESCRIPTION

5.70 See Figure 7—3 for the functional schematic diagram of the interrupt and display function. Separate descriptions of the address decoding, interrupt generation, and display updating subfunctions are presented in the following paragraphs.

5.71 ADDRESS DECODER

5.72 The address decoding utilizes certain memory address locations placed on the address bus by the software to control the events occurring during the interrupt and display function.

5.73 Address bits AØ through A4 and A8 through A15, in conjunction with control lines HLDA and $\overline{\text{MEMW}}$, are used for address decoding. These are all outputs of CPU U9 and system controller U7 located on A8. The hold function of U9 is not used by the 1260 and, therefore, the HLDA output of U9 is always in the non-active or low state. This is used to permanently enable tri-state bus drivers U4, U5, and U6.

5.74 Address bits A8 through A15 are buffered by U5 and U6 and then applied to open collector AND gates U2A, U2B, and U2C. When A8 through A15 are all high, the AND gate output goes high, is buffered by U4, and appears as an output line designated I/O. This corresponds to memory locations FFXXH and has been chosen to enable the I/O ports used in the 1260. The remaining five bits are buffered in U4 and U5 and are then designated ABØ through AB4. They form the XX parts of the general FFXXH locations. The final line used in decoding is $\overline{\text{MEMW}}$ that is present at the output of U7 anytime there is a write command.

5.75 Address decoder U16 is a device that has two enable inputs and three binary inputs. When the G1 enable is high and the G2A/B input is low, the Y outputs go low one at a time in accordance with the binary input code. Table 5—4 shows how these inputs are decoded to form FFØ3H(W) and FFØ4H(W).

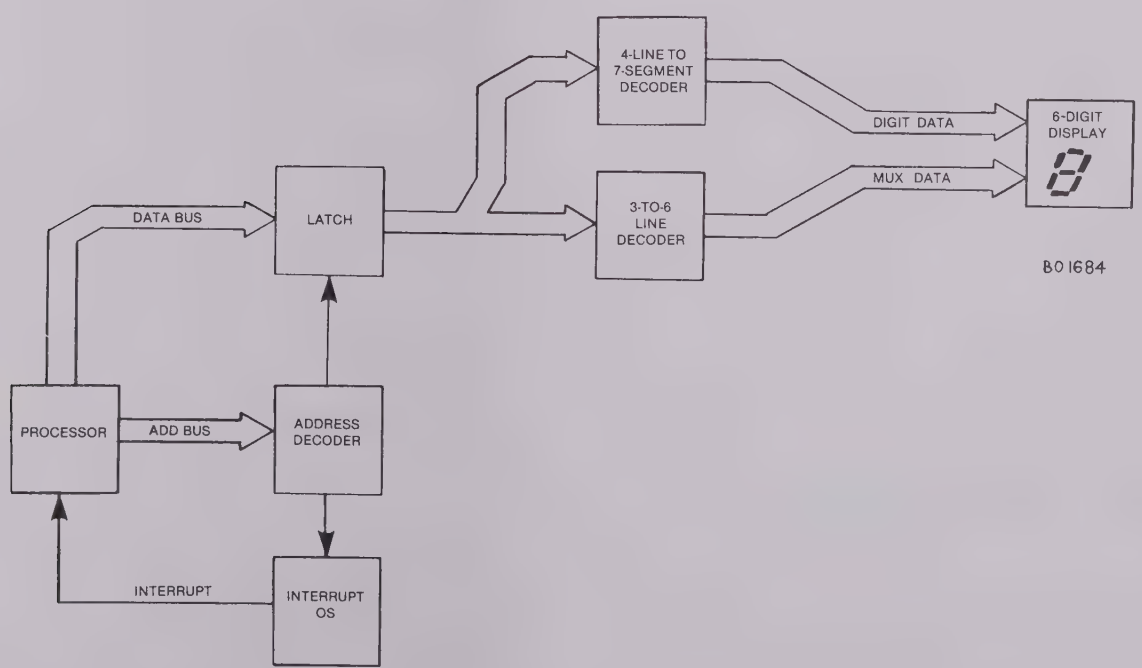


Figure 5—7. Interrupt And Display Section, Simplified Block Diagram

Table 5—4. Interrupt And Display Address Decoding Truth Table

$\overline{MEMW}$	I/O	AB4	AB3	AB2	AB1	ABØ	FFØ3H(W)	FFØ4H(W)
L	H	L	L	L	H	H	L	H
L	H	L	L	H	L	L	H	L

5.76 INTERRUPT GENERATION

5.77 In the 1260, the interrupt cycle is self perpetuating and is designed to occur once per millisecond. Whenever an interrupt command is generated, the processor enters an interrupt mode and the main program vectors to an interrupt service routine. During the execution of this service routine, the transmitter, receiver, and the dial keypad are serviced, if they request it, and the display is updated.

5.78 The interrupt cycle gets its start at power-on, at which time a reset command is generated. The most convenient starting point at which to begin discussion of the interrupt cycle is to assume that it is presently in the interrupt mode. This is represented by a low $\overline{INTR}$ line at the $\overline{Q}$ output of U13A. See Figure 5—8 for the interrupt cycle event sequence diagram.

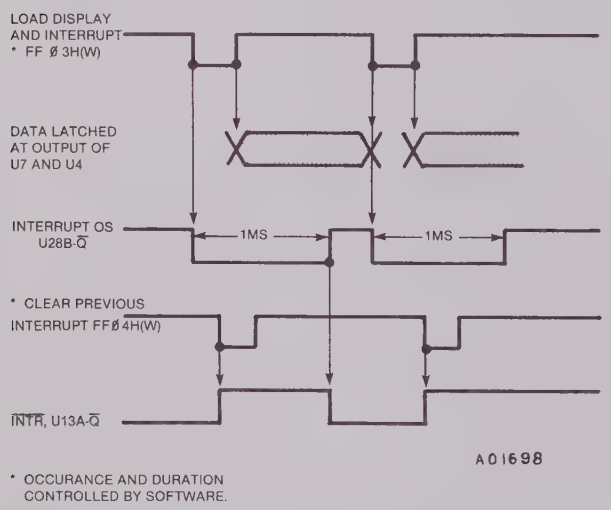

LOAD DISPLAY AND INTERRUPT * FF Ø 3H(W)
DATA LATCHED AT OUTPUT OF U7 AND U4
INTERRUPT OS U28B-Q
1MS
1MS
* CLEAR PREVIOUS INTERRUPT FFØ4H(W)
INTR, U13A-Q
A01698
* OCCURANCE AND DURATION CONTROLLED BY SOFTWARE.

Figure 5—8. Event Sequence Diagram For The Interrupt And Display Function

5.79 While the processor is executing the interrupt service routine, a write command to memory location FFØ3H is given. This is decoded and appears as FFØ3H(W) at the trigger input to one-shot U28B. The negative leading edge triggers the one-shot, which requires 1 millisecond to time out. During this time, the subroutine issues a write command to memory location FFØ4H. This is decoded and, as FFØ4H(W), clears the previous interrupt by clearing U13A. At the end of 1 millisecond, the positive edge of the one-shot output clocks U13A and the $\overline{INTR}$ line goes low to again place the processor in the interrupt mode. The appearance of the next FFØ3H(W) signal triggers the one-shot and the cycle repeats.

5.80 DISPLAY UPDATING

5.81 The eight data bits at the D outputs of U9 on A8 are buffered in system controller U7 and then placed on the data bus. Bits DBØ through DB3 carry the character information in binary format. The muliplex information in binary format is represented by DB4, DB5, and DB6.

5.82 Tri-state bus drivers U10 and U1 located on A7 are permanently enabled since their $\overline{G}1/2$ inputs are strapped to ground. Thus whatever is present on the data bus is always present at the inputs to latches U7 and U4. Approximately once each millisecond, FFØ3H(W) goes low for a short period of time. The leading edge of this signal allows data to enter U7 and U4 but is not latched and thus is not yet present at the outputs. When FFØ3H(W) returns to the high state, the data is latched and applied to U8 and U7 located on A11A2.

5.83 The 4-line to 7-segment decoder U8 converts the 4-line BCD input data to a 7-segment code that determines the character to be displayed. See Table 5—5. The decoder outputs are applied through current limiting resistors to the six LED displays in parallel.

5.84 The particular LED display to be lighted at any instant is the function of 3-line to 6-line multiplex decoder U7. The 3-line binary input causes the outputs to go low one at a time as shown in Table 5—6. The selected low output saturates its associated transistor and +5 Vdc is applied to the corresponding LED display. Each LED display is turned on for 1 millisecond and turned off for 5 milliseconds. This reduces the current drain on the +5 Vdc power supply. Decimal points are permanently lighted by strapping the DP inputs to ground through current limiting resistors.

Table 5—5. 4-Line To 7-Segment Decoding Truth Table

DISPLAY	U8										
	D	C	B	A	a	b	c	d	e	f	g
0	L	L	L	L	L	L	L	L	L	L	H
1	L	L	L	H	H	L	L	H	H	H	H
2	L	L	H	L	L	L	H	L	L	H	L
3	L	L	H	H	L	L	L	L	H	H	L
4	L	H	L	L	H	L	L	H	H	L	L
5	L	H	L	H	L	H	L	L	H	L	L
6	L	H	H	L	H	H	L	L	L	L	L
7	L	H	H	H	L	L	L	H	H	H	H
8	H	L	L	L	L	L	L	L	L	L	L
9	H	L	L	H	L	L	L	H	H	L	L

Table 5—6. 3-Line To 6-Line Multiplex Decoder Truth Table

DIGIT ON	U7								
	C	B	A	YØ	Y1	Y2	Y3	Y4	Y5
PPSX10^{1}	L	L	L	L	H	H	H	H	H
PPSX10^{0}	L	L	H	H	L	H	H	H	H
PPSX10^{-1}	L	H	L	H	H	L	H	H	H
%BKX10^{1}	L	H	H	H	H	H	L	H	H
%BKX10^{0}	H	L	L	H	H	H	H	L	H
%BKX10^{-1}	H	L	H	H	H	H	H	H	L

5.85 DIAL KEYPAD DATA ENTRY FUNCTION BLOCK DIAGRAM DESCRIPTION

5.86 See Figure 5—9 for a simplified block diagram of the dial keypad functional section. The purpose of this functional section is to convert 1-out-of-10 data supplied by the dial keypad into BCD data that is then placed on the data bus, for use by the processor.

5.87 When any of the dial keypad pushbuttons is pressed, the 1-out-of-10 data is converted to BCD data in an encoder. The encoder output is used to generate a keypad flag and to latch itself into the I/O port. Software now takes control to read the flag, place the data on the bus, and clear the flag at the completion of the cycle. Software control is exercised through the process of decoding certain memory addresses.

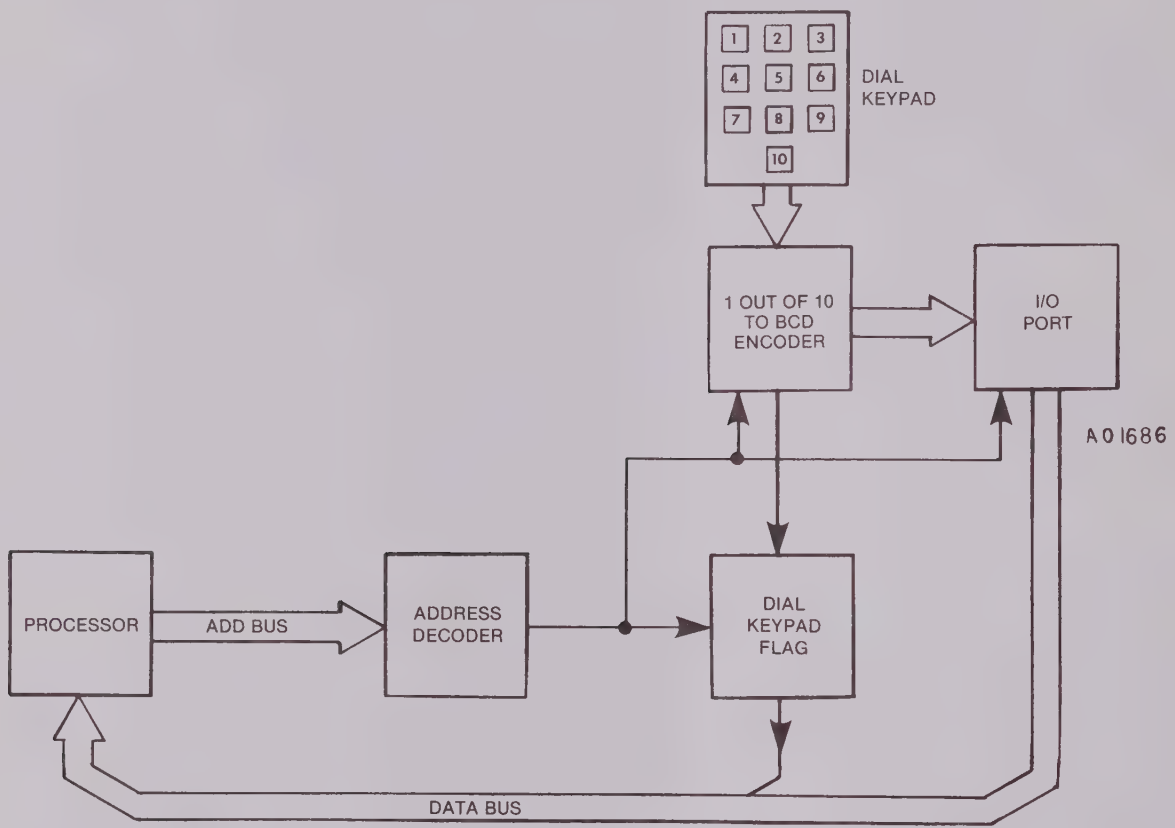


Figure 5—9. Dial Keypad Data Entry Functional Section, Simplified Block Diagram

5.88 DIAL KEYPAD DATA ENTRY FUNCTION DETAILED CIRCUIT DESCRIPTION

5.89 See Figure 7—4 for the functional schematic diagram of the dial keypad data entry function. Figure 5—10 illustrates the sequence of events that occur during the processing of dial keypad data onto the bus. Table 5—7 is a truth table for address decoding and Table 5—8 is a truth table for the 1-out-of-10-to-BCD encoding scheme.

5.90 Dial keypad S17 is a 1-out-of-10 device with the selected line at ground. The selected line is then immediately converted to 4-line BCD by priority encoders U19 and U20 located on A7. All inputs are connected to +5 Vdc through pull-up resistors. Priority encoder outputs are active low as shown on the truth table.

5.91 BCD data is applied to the inputs of U22 through U21A, B, and D. Any time a pushbutton is pressed, the output of U21C immediately goes high and triggers 50-millisecond one-shot U30B. The trailing edge of the Q output latches the BCD data into U22 but the data is not yet placed on the bus. The trailing edge of the Q output clocks U32A and, if the output of U21C is still high, the flag flip flop is set and its Q output goes high.

5.92 Approximately once each millisecond, FFØDH(R) goes low and U25A places the flag on the data bus via D7. When the controller is ready to receive the keypad data, FFØEH(R) goes low and this is inverted by U35B to enable the outputs of I/O port U22. The BCD data is now on the data bus. After the controller has finished with the keypad data, FFØFH(R) goes low to clear flag flip flop U32A and the cycle is now complete.

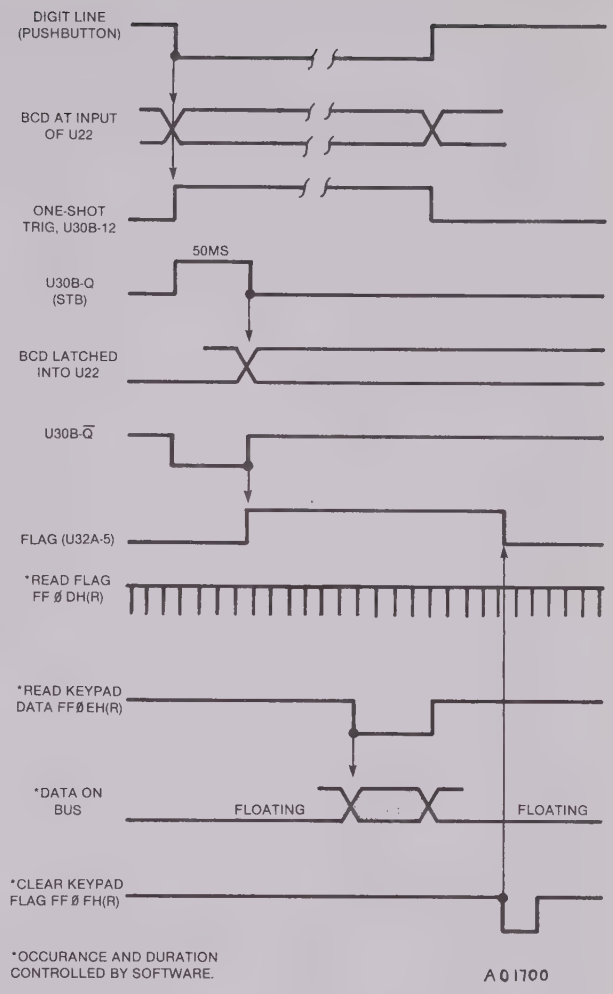


Figure 5—10. Event Sequence Diagram For The Dial Keypad Data Entry Function

Table 5—7. Dial Keypad Data Entry Address Decoding Truth Table

$\overline{\text{MEMR}}$	I/O	AB4	AB3	AB2	AB1	ABØ	FFØDH(R)	FFØEH(R)	FFØFH(R)
L	H	L	H	H	L	H	L	H	H
L	H	L	H	H	H	L	H	L	H
L	H	L	H	H	H	H	H	H	L

Table 5—8. 1-Out-Of-10 To BCD Encoding Truth Table

DIGIT	U19			U20				U22			
	AØ	A1	A2	AØ	A1	A2	EØ	DI1(1)	DI3(2)	DI4(4)	DI2(8)
1	L	H	H	H	H	H	L	H	L	L	L
2	H	L	H	H	H	H	L	L	H	L	L
3	L	L	H	H	H	H	L	H	H	L	L
4	H	H	L	H	H	H	L	L	L	H	L
5	L	H	L	H	H	H	L	H	L	H	L
6	H	L	L	H	H	H	L	L	H	H	L
7	L	L	L	H	H	H	L	H	H	H	L
8	H	H	H	H	H	H	H	L	L	L	H
9	H	H	H	L	H	H	H	H	L	L	H
0	H	H	H	H	L	H	H	L	H	L	H

5.93 **SWITCH STATUS FUNCTION BLOCK DIAGRAM DESCRIPTION**

5.94 See Figure 5—11 for a simplified block diagram of the switch status function. The purpose of this function is to keep the processor informed of the status of the MAX, MIN, ON HOOK/OFF HK-DIAL/CONT, SPEED, and % BREAK switches. When the processor is ready to poll a particular switch, a corresponding address is placed on the address bus. This is decoded in an address decoder which enables the bus driver associated with the switch of interest. The data bus carries the information to the processor where it is used.

5.95 **SWITCH STATUS FUNCTION DETAILED CIRCUIT DESCRIPTION**

5.96 See Figure 7—5 for the functional schematic diagram of the switch status function. This function consists of the address decoder and a bus driving system described in the following paragraphs.

5.97 ADDRESS DECODER

5.98 The address decoder utilizes certain memory address locations placed on the address bus by the software to control the events occurring during the process of monitoring the switch status. Address bits AØ through A4 and A8 through A15, in conjunction with control lines HLDA and $\overline{\text{MEMR}}$ are used for address decoding. These are all outputs of CPU U9 and system controller U7 located on A8. The hold function of U9 is not used by the 1260 and, therefore, the HLDA output of U9 is always in the non-active or low state. This is used to permanently enable tri-state bus drivers U4, U5, and U6.

5.99 Address bits A8 through A15 are buffered by U5 and U6 and then applied to open collector AND gates U2A, U2B and U2C. When A8 through A15 are all high, the AND gate output goes high, is buffered by U4, and appears as an output line designated I/O. This corresponds to memory locations FFXXH and has been chosen to enable the I/O ports used in the 1260. The remaining five bits are buffered in U4 and U5 and are then designated ABØ through AB4. They form the XX parts of the general FFXXH locations. The final line used in decoding is $\overline{\text{MEMR}}$ that is present when there is a read command.

5.100 Address decoder U2 located on A6 is a device that has two enable inputs and three binary inputs. When the G1 enable is high and the G2A/B enable is low, the Y outputs go low one at a time in accordance with the binary inputs. Table 5—9 shows how these inputs are decoded to form the four decodes.

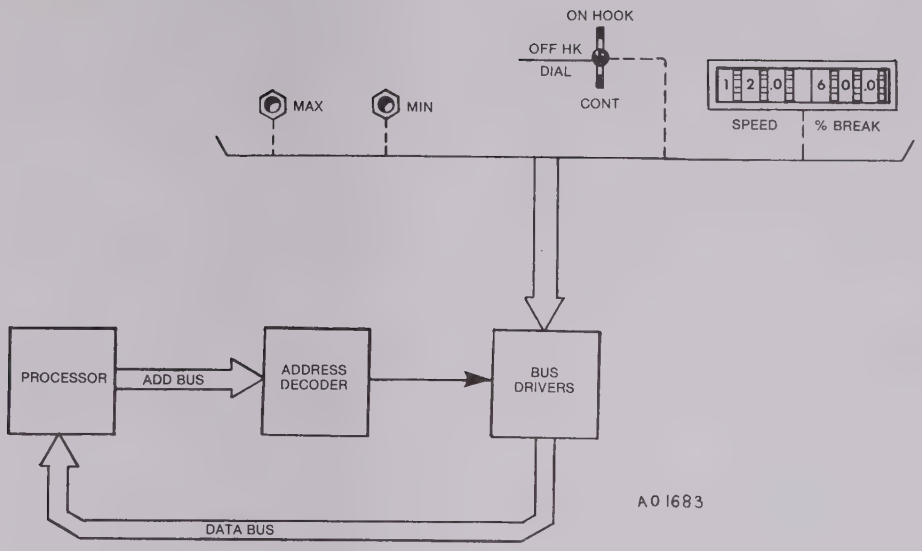


Figure 5—11. Switch Status Functional Section, Simplified Block Diagram

Table 5—9. Switch Status Address Decoding Truth Table

I/O	$\overline{\text{MEMR}}$	AB0	AB1	AB2	AB3	AB4	FFXXH(R)	READ SWITCH STATUS FOR
H	L	H	H	L	L	H	FF13H(R)	ON HOOK/OFF HK-DIAL/CONT, MIN and MAX
H	L	L	L	H	L	H	FF14H(R)	% BREAK X 10^1 and X 10^0
H	L	H	L	H	L	H	FF15H(R)	% BREAK X 10^{-1} and PPS X 10^{-1}
H	L	L	H	H	L	H	FF16H(R)	PPS X 10^1 and X 10^0

5.101 LINE DRIVERS

5.102 See Figure 7—5 for the functional schematic diagram of the switch status function. The SPEED and % BREAK thumbwheel switches located on the front panel provide BCD outputs. The active lines are grounded and the others are open. The MIN, MAX, and the ON HOOK/OFF HK-DIAL/CONT switches apply ground to the selected line. All of these lines are hard wired to tri-state bus drivers located on A6. All of the bus driver inputs, including unused inputs, are tied to the +5 Vdc supply through pull-up resistors.

5.103 When a low level select gate is applied to the bus drivers, the BCD information is placed on an internal data bus and then on the general data bus through isolation resistors. Selection of which switch gets read onto the data bus is under control of the software and is accomplished by decoding memory addresses.

5.104 **RESET AND MONITOR FUNCTION BLOCK DIAGRAM DESCRIPTION**

5.105 See Figure 5—12 for a simplified block diagram of the reset and monitor function. As seen on the illustration, there are two separate functions represented: (1) reset, and (2) monitor.

5.106 The purpose of the reset function is to get the software running in synchronization with the hardware; particularly when power is first applied to the set. There are three ways in which to generate a reset pulse at the input to the processor. The first (and most common) is by the power-on detector whenever the POWER switch is set to the ON position. The second is via the monitor sensor and the reset one-shot whenever the E&M/MON/LOOP switch is set to (or passes through) the MON position. In this case, the reset function is used as a convenient means of clearing the digital displays

This ensures that, when switching from LOOP to E&M or vice versa, any data displayed is a result of a measurement taken in the new switch position and not stale data from an old measurement. The third and last method of generating a reset pulse is by pressing an internally-mounted reset switch. This switch is provided simply as a convenience for troubleshooting. In all three cases, the reset pulse is used by the processor and an associated bootstrap flip flop to initialize the program.

5.107 The purpose of the monitor circuits is to visually display the signaling activity at the parallel-connected RCV and SEND jacks before beginning a test and to visually display the signal activity being received and being transmitted during a test.

5.108 When the E&M/MON/LOOP switch is set to the MON position, the RCV and SEND jacks are connected in parallel. The tips are brought to one opto isolator and the rings to another. The output of the monitor sensor allows the outputs of the opto isolators to control indicators DS1 and DS2. A lighted indicator indicates an on hook condition. An off hook is shown by indicators that are not lighted. When the E&M/MON/LOOP switch is in either the E&M or the LOOP position, the gates pass the receiver and transmitter outputs to control indicators DS1 and DS2. The on hook and off hook indications are the same as when monitoring the jacks.

5.109 RESET AND MONITOR FUNCTION DETAILED CIRCUIT DESCRIPTION

5.110 See Figure 7—6 for the functional schematic diagram of the reset and monitor functions.

5.111 RESET CIRCUIT

5.112 There are three conditions for the reset pulse at the $\overline{\text{RESIN}}$ input pin 2 of clock generator U8 located on A8. The first condition is that generated by RC network R4-C8. When power is first applied, the +5 Vdc comes up immediately, but C8 charges slowly through R4. This allows the Schmitt trigger input of U8 to internally generate a reset pulse.

5.113 The second condition for a reset pulse occurs when S2 is set to (or passes through) the MON position. This grounds one side of R73 on A6 and lowers the input to U1D. The rising edge of the U1D output triggers 50-millisecond one-shot U15B, which produces a negative pulse at its output. This is applied through CR13 and R76 again to the $\overline{\text{RESIN}}$ input of the clock generator.

5.114 The third way of producing a reset pulse is to momentarily press S1 on A8. As a result of any one of these three reset pulses, U8 provides a positive edge at the RESET output pin 1.

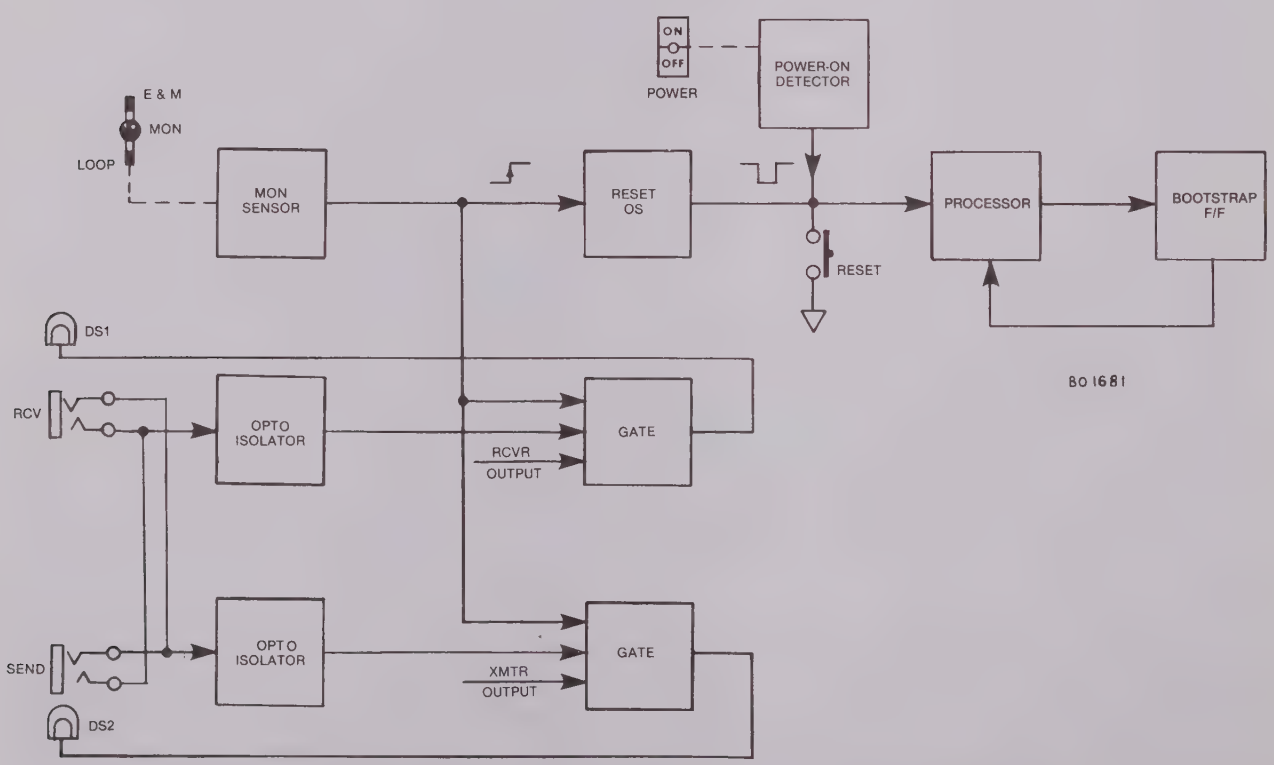


Figure 5—12. Reset And Monitor Functional Section, Simplified Block Diagram

5.115 Any reset pulse immediately causes CPU U9 to attempt to read the first instruction stored in memory. To do this the CPU places address code ØØØØH on the address bus. This is the first memory location in RAM but, it is desired to read the first instruction stored in PROM U9. This is done by momentarily forcing the address decoder located on the memory board to decode memory location 8ØØØH, which is the first location in PROM U9. This memory location contains an instruction that gets the program started.

5.116 The same positive edge at the RESET output of clock generator U8 is inverted by U3C and applied to the bootstrap flip flop located on A9. The bootstrap is set and its output goes positive. This then becomes a substitute for AB15, the most significant bit of the address, and is applied through U5D to the SEL B input of U6. Along with AB10 through AB15, all of which are low, the SEL B input causes the 2Y2 output to go low and select PROM U9. Since ABØ through AB9 are all low, the cumulative effect is that the instruction stored in memory location 8ØØØH is placed on the data bus and applied to the CPU.

5.117 Now that the CPU has been given a reliable instruction to start the program, it is necessary to free up the operation of AB15 at the input to U5D on A9. After executing further instructions, the CPU causes system controller U7 to issue a $\overline{\text{MEMW}}$ write command. This low level resets the bootstrap flip flop, whose output goes low and frees AB15 so that this bit has control when required. The bootstrap remains in this state until another reset pulse is generated by any of the methods described previously.

5.118 MONITOR CIRCUIT

5.119 Indicators DS1 and DS2 provide a visual indication of the activity at J1 and J2 when S2 is in the MON position and of the receiver and transmitter circuits when S2 is in either the E&M or LOOP position.

5.120 First consider operation when S2 is in the MON position. Contacts of S2 apply ground to one side of R73 on A6. The resulting low level at the input of U1D is also applied to inputs of U16A and U16D to inhibit the transmitter and receiver outputs. The high level at the output of U1D enables one input each of U15B and U16C. Two other sets of S2 contacts connect the tip and ring of J1 to the tip and ring of J2. A third set of contacts connects the jacks to level detectors Q2 and Q3 located on A6.

5.121 If the ring is either open or ground, Q3 is cut off and the output of U18 appears like a high input to U16C. With the other input high, the output of U16C goes low and lights DS2. If the ring is at battery, both Q3 and U18 conduct. This grounds the input to U16C and its output is high, which keeps DS2 from being lighted.

5.122 If the tip is at battery or open, Q2 is cut off and U17 does not conduct. This places the input of U16B high. Along with the other high input, the output of U16B goes low and lights DS1. When the tip is grounded, both Q2 and U17 conduct. This grounds the input of U16B so that its output goes high and keeps DS1 from being lighted.

5.123 When S2 is in either the E&M or the LOOP position, the input of U1D is pulled up through R31. This high level enables the inputs of U16D and U16A. The low outputs of U1D inhibits U16C and U16B. When the transmitter output is on hook, the output of U16D goes low to light DS2. When the receiver output is on hook, the output of U16A goes low to light DS1.

SECTION 6

CALIBRATION

6.1 This section includes a set of calibration instructions.

6.2 There are two adjustments in the receiver section and one in the transmitter section. The receiver must be calibrated first since it is used to calibrate the transmitter. For this reason, follow the instructions exactly as presented. To calibrate the Model 1260, perform the following steps.

1. Remove the four screws located on the rear panel and then slide the cover off.

2. Connect a 48-volt supply to the 48V jack located on the rear panel. The tip must be −48 Vdc and the sleeve ground.

3. Connect a variable power supply and a Digital Multimeter (DMM) to cord equipped with a 310-type plug on one end. The tip must be positive with respect to the ring. See Figure 6−1 for a typical calibration setup. Insert the plug into the RCV jack.

4. Set the E&M/MON/LOOP switch to LOOP and the RECEIVE mode switch to WET LOOP.

5. On analog receiver board A6, adjust R42 and R45 fully clockwise. See Figure 6−2 for the location of these adjustments.

6. Adjust the power supply voltage to obtain an indication of 9.00 ± 0.25 Vdc on the DMM.

7. Set the 1260 POWER switch to OFF and then return it to ON. This resets the processor and ensures that all circuitry gets started in the correct sequence.

8. Slowly adjust R42 until the front panel meter needle jumps to the OFF HK position at the far right.

9. Adjust the power supply voltage to obtain an indication of 2.50 ± 0.25 Vdc on the DMM.

10. Slowly adjust R45 until the front panel meter needle jumps to the ON HK position at the far left.

11. Repeat steps 6 through 10 until no further adjustment is required. This is indicated when 9 Vdc causes the meter needle to go OFF HK and 2.5 Vdc causes it to go ON HK. If the critical points are approached carefully during the first adjustment sequence, the end point should be reached within three repetitions of the adjustments.

12. Remove the variable power supply and the DMM.

13. Loop the transmitter and receiver by interconnecting the SEND and RCV jacks using a cord equipped with 310 plugs on both ends.

14. Set the BRIDGE/TERM switch to TERM.

15. Set the RECEIVE and SEND mode switches to DRY LOOP.

16. Set the ON HOOK/OFF HK-DIAL/CONT switch to CONT.

17. Release all LOOP RES and LINE LEAK switches.

18. Set the SEND SPEED thumbwheel switches to 20.0 and the % BREAK thumbwheel switches to 60.0.

19. On A11A4, adjust R1 (Figure 6−2) to obtain a front panel % BREAK indication of 60.0.

20. Disconnect power and replace the cover.

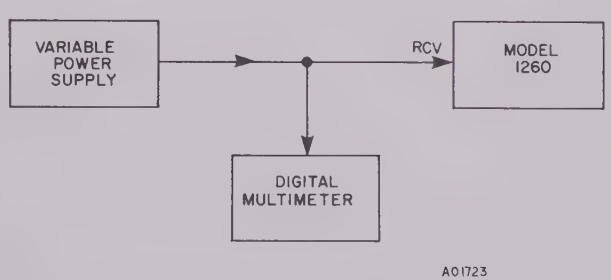


Figure 6−1. Typical Model 1260 Calibration Test Setup

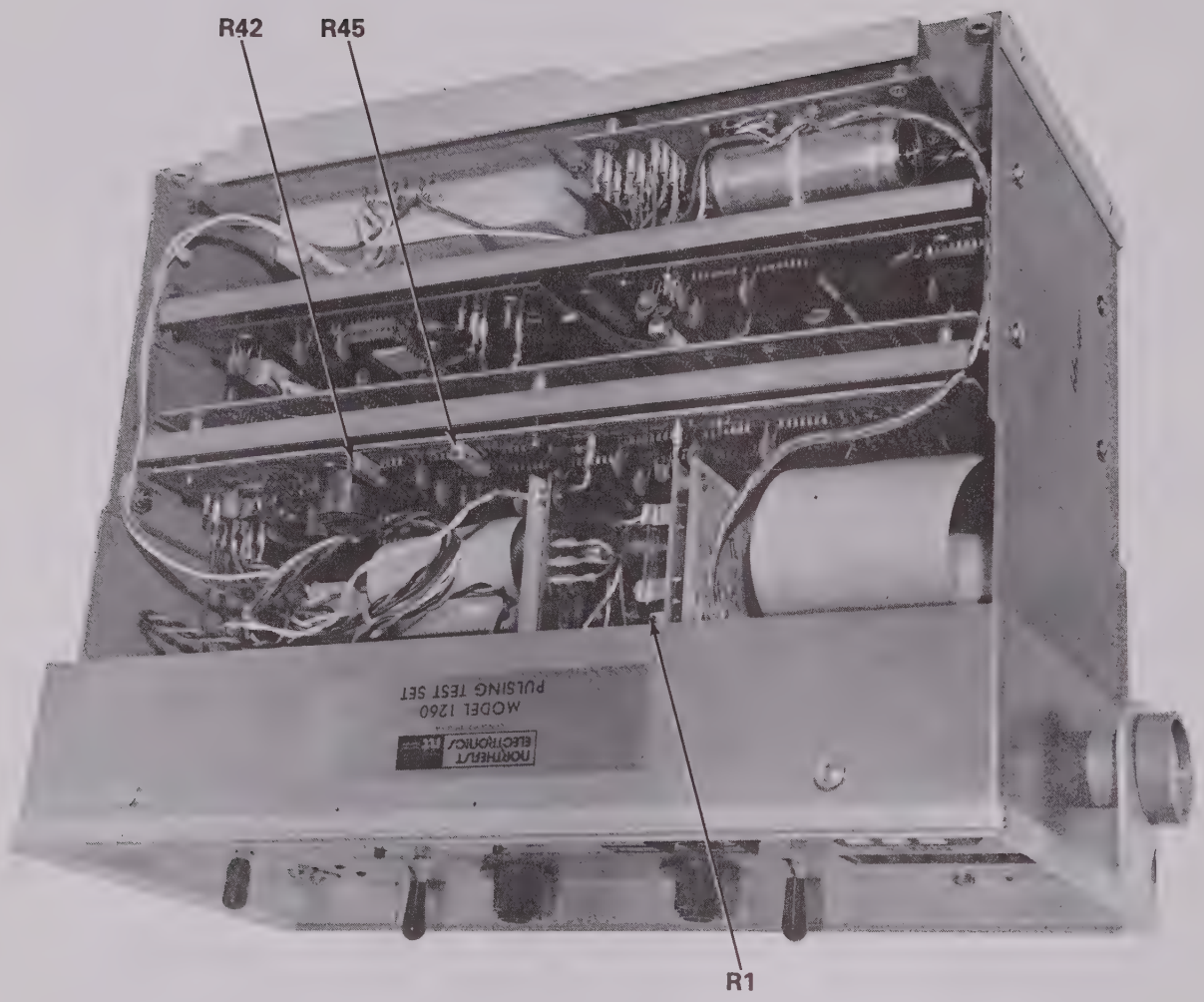
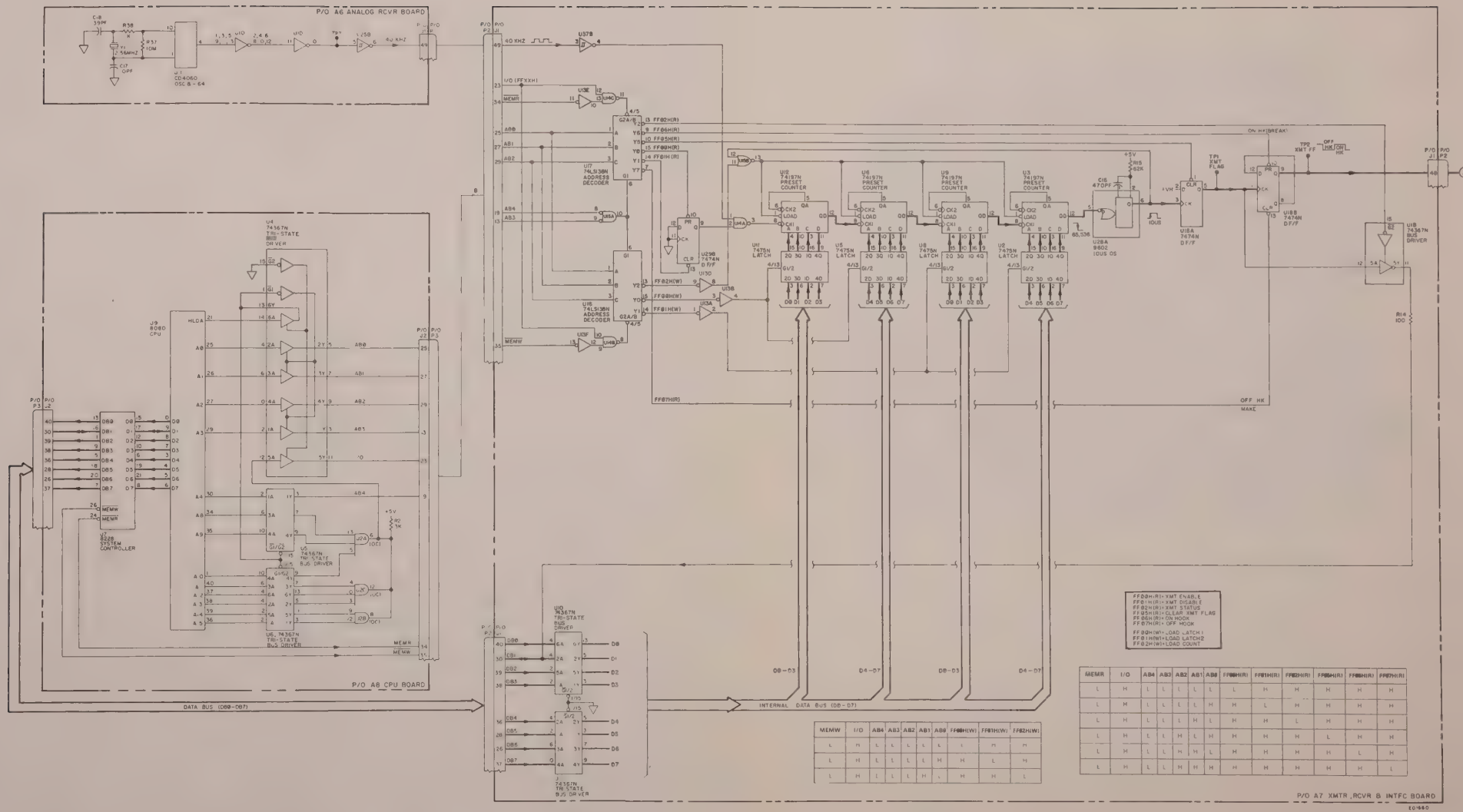


Figure 6—2. Model 1260 Calibration Adjustment Locations

SECTION 7

DIAGRAMS

7.1 This section contains functional, parts location, and schematic diagrams for the Model 1260.


P/O A6 ANALOG RCVR BOARD
P/O A8 CPU BOARD
P/O A7 XMTR ,RCVR & INTFC BOARD
DATA BUS (D0-D7)
INTERNAL DATA BUS (D0-D7)
U9 8080 CPU
U4 74367N TRI-STATE BUS DRIVER
U6 74367N TRI-STATE BUS DRIVER
U10 74367N TRI-STATE BUS DRIVER
U7 74LS138N ADDRESS DECODER
U18 74LS138N ADDRESS DECODER
U12 74197N PRESET COUNTER
U6 74197N PRESET COUNTER
U9 74197N PRESET COUNTER
U3 74197N PRESET COUNTER
U1 7475N LATCH
U5 7475N LATCH
U8 7475N LATCH
U2 7475N LATCH
U8 74367N BUS DRIVER
U28A 9602 1DUS 0S
U18A 7474N D F/F
U18B 7474N D F/F
U29B 8228 SYSTEM CONTROLLER
U29A
U5 74367N TRI-STATE BUS DRIVER
U29B 74367N TRI-STATE BUS DRIVER
U37B
U3E
U3F
U3C
U3D
U3B
U3A
U29B 7474N D F/F
U15
U16
U17
U1
U2
U3
U4
U5
U6
U7
U8
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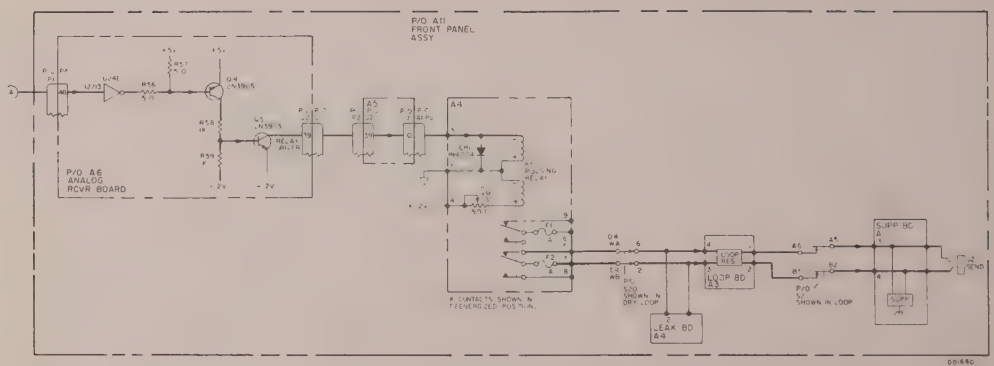
U3F
U15
U16
U17


P/O A11
FRONT PANEL
ASSY
P/O A6
ANALOG
RCVR BOARD
A4
A5
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
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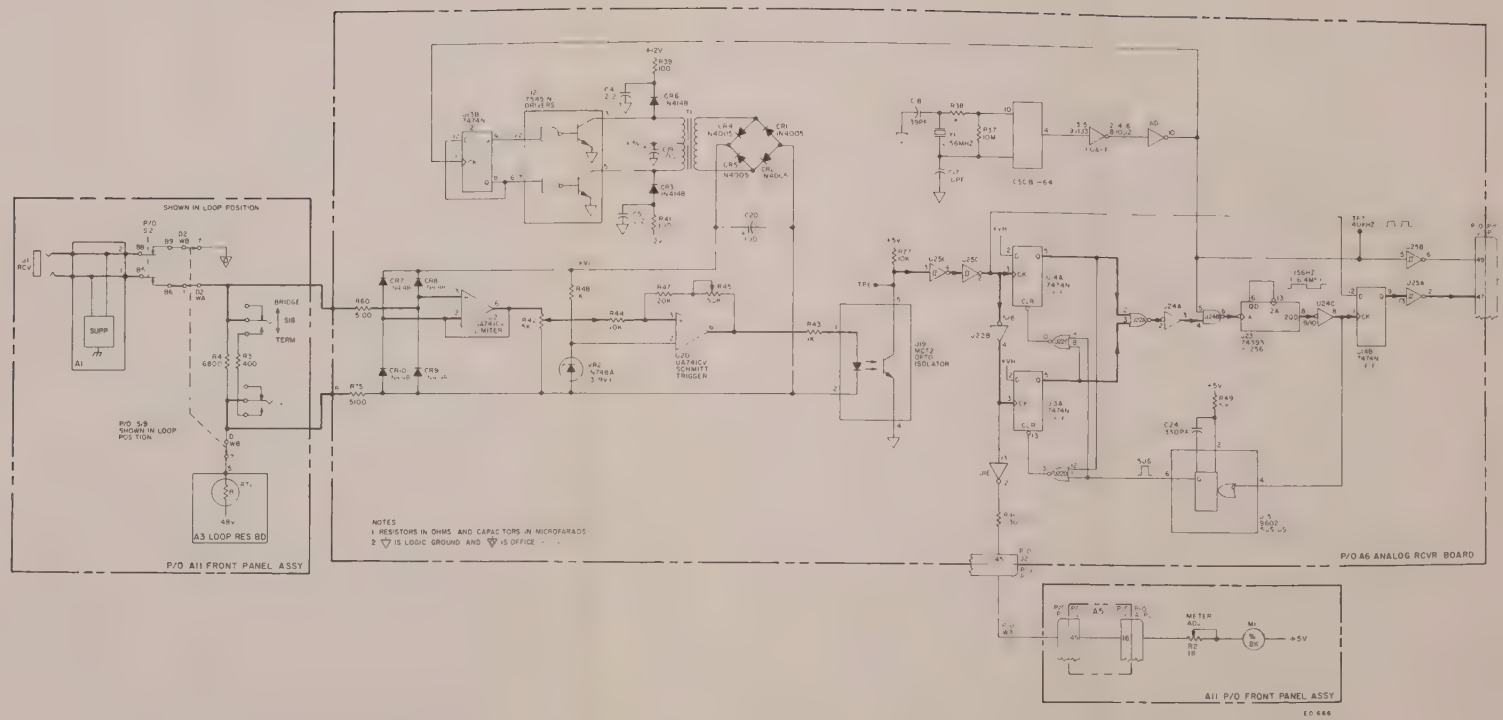
A46


SHOWN IN LOOP POSITION
P/O S2
SUPP
A1
BRIDGE
TERM
SIB
P/O S9 SHOWN IN LOOP POSITION
A3 LOOP RES BD
P/O A11 FRONT PANEL ASSY
+12V
+5V
CR6 N4148
CR1 IN4005
CR4 N4005
CR5 N4305
CR3 N4148
CR7 N4148
CR8
CR10
CR9
U20 LM741CV SCHMITT TRIGGER
U19 MCT2 OPTO ISOLATOR
TP1
U25A
U25B
U25C
U24A 7474N
U24B 7474N
U24C 7474N
U23 74193
U22A 7474N
U22B
U13A 7474N
U13B
U13C 9602
U5
U4
U3
U2
U1
Y1 16MHz
CSCB-64
C26 150PF
R49
R50
R51
R52
R53
R54
R55
R56
R57
R58
R59
R60
R61
R62
R63
R64
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R87
R88

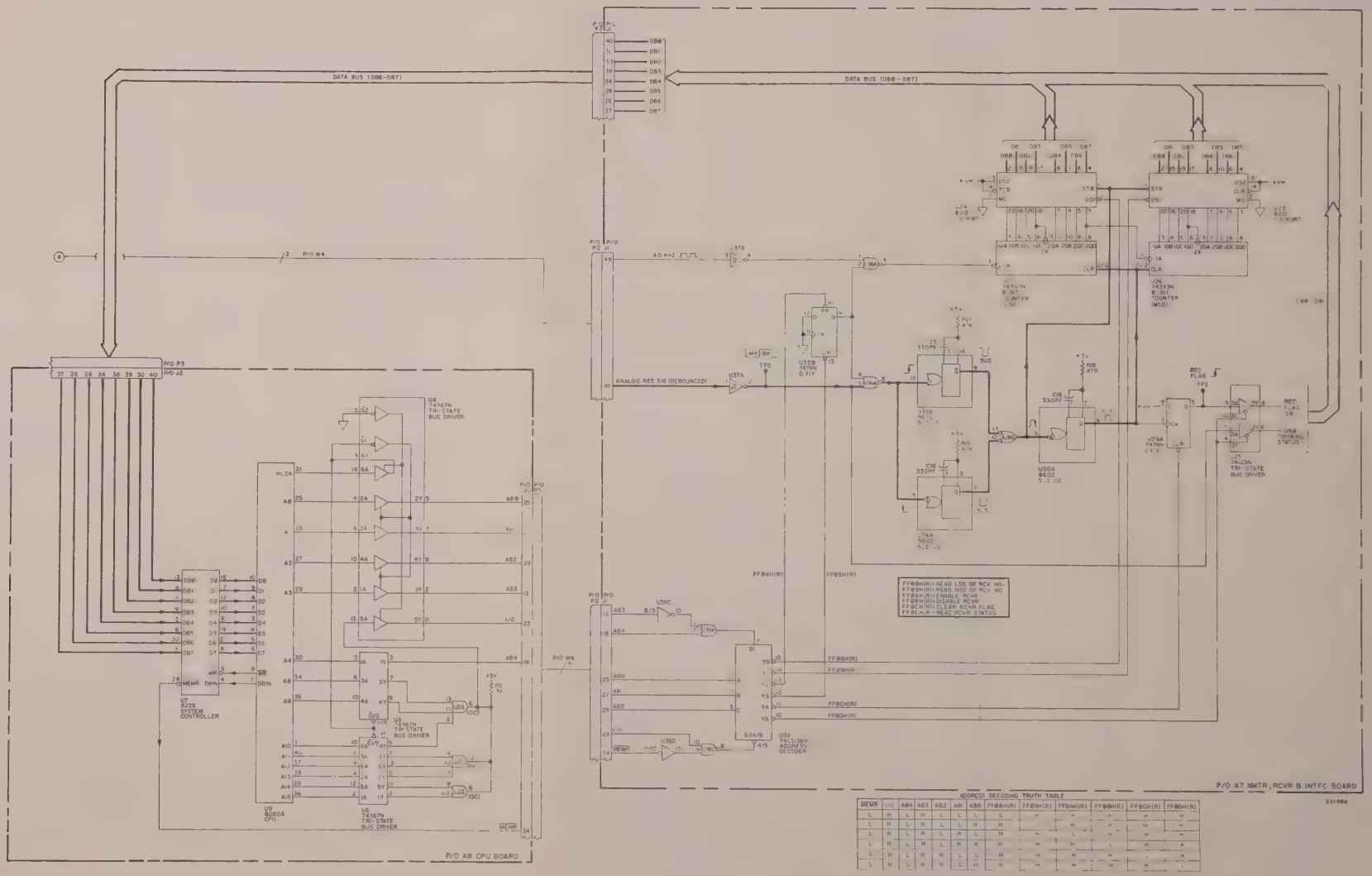


Figure 7—2. Receiver Functional Schematic Diagram (Sheet 2 of 2)

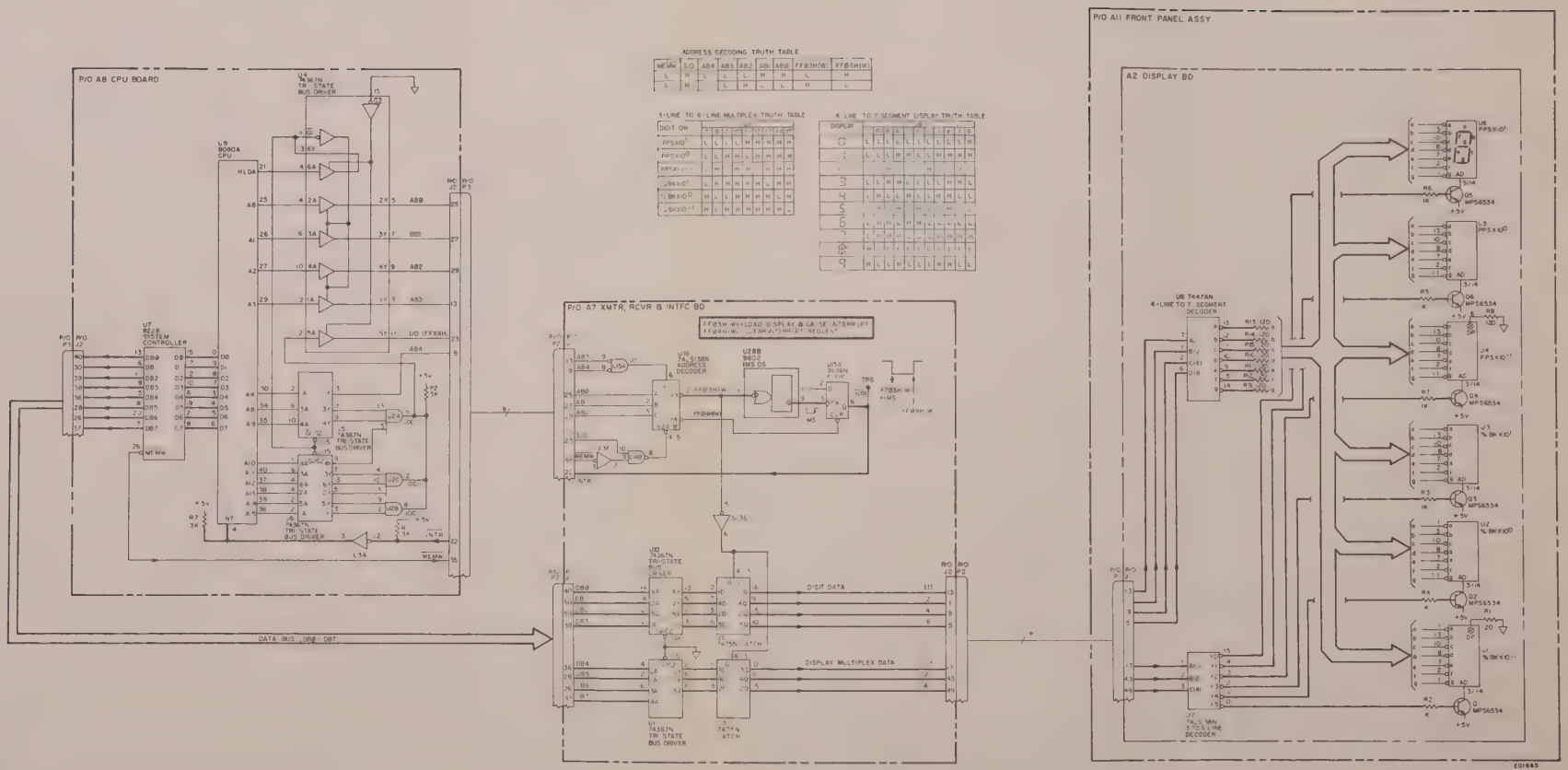

P/O A8 CPU BOARD
P/O A7 XMTR, RCVR & INTFC BD
P/O A11 FRONT PANEL ASSY
A2 DISPLAY BD
ADDRESS DECODING TRUTH TABLE
4-LINE TO 6-LINE MULTIPLEX TRUTH TABLE
4 LINE TO 7 SEGMENT DISPLAY TRUTH TABLE
DATA BUS, DB0 - DB7
DIGIT DATA
DISPLAY MULTIPLEX DATA
E01665

Figure 7—3. Interrupt And Display Functional Schematic Diagram

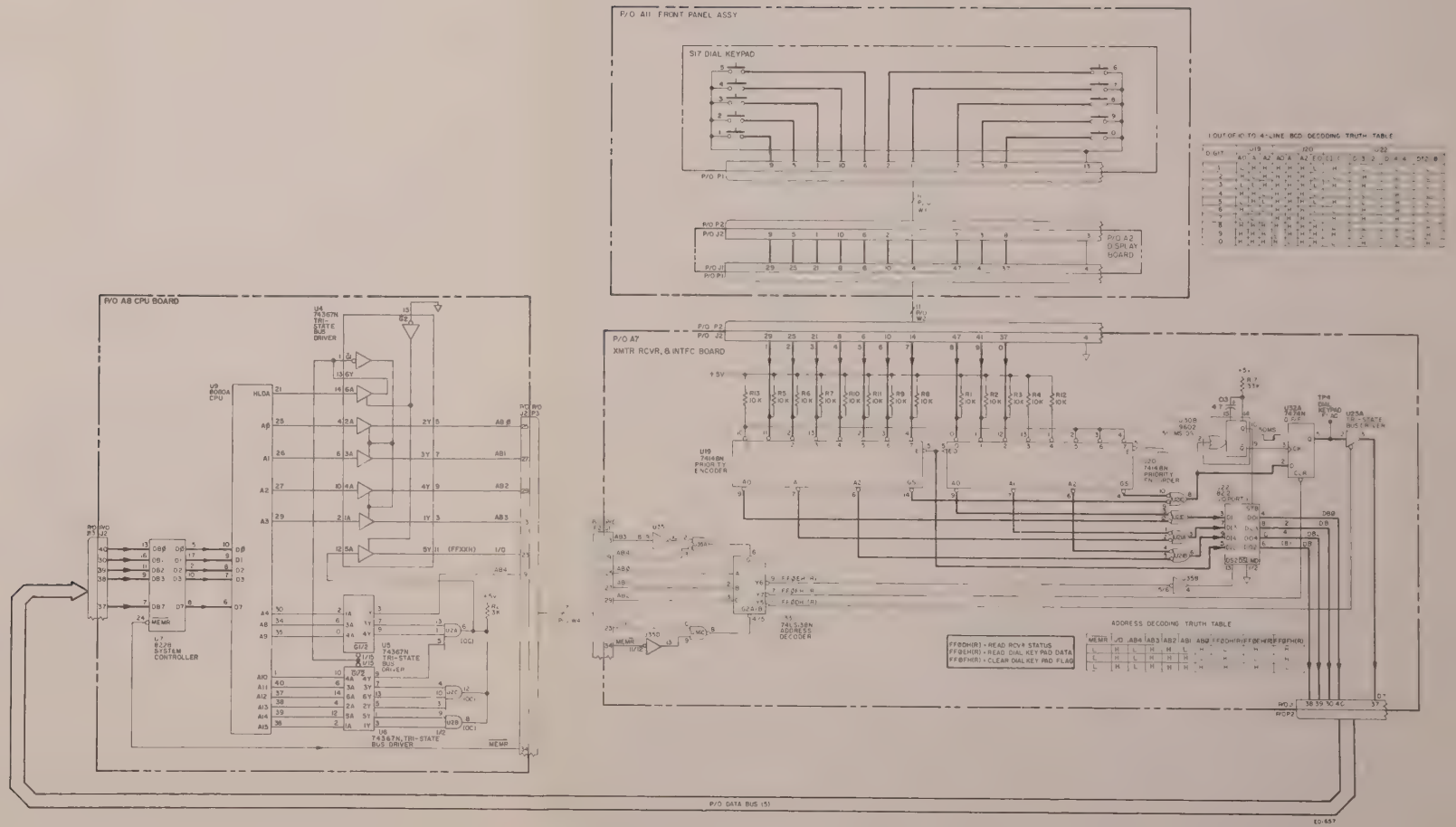


Figure 7—4. Dial Keypad Data Entry Functional Schematic Diagram

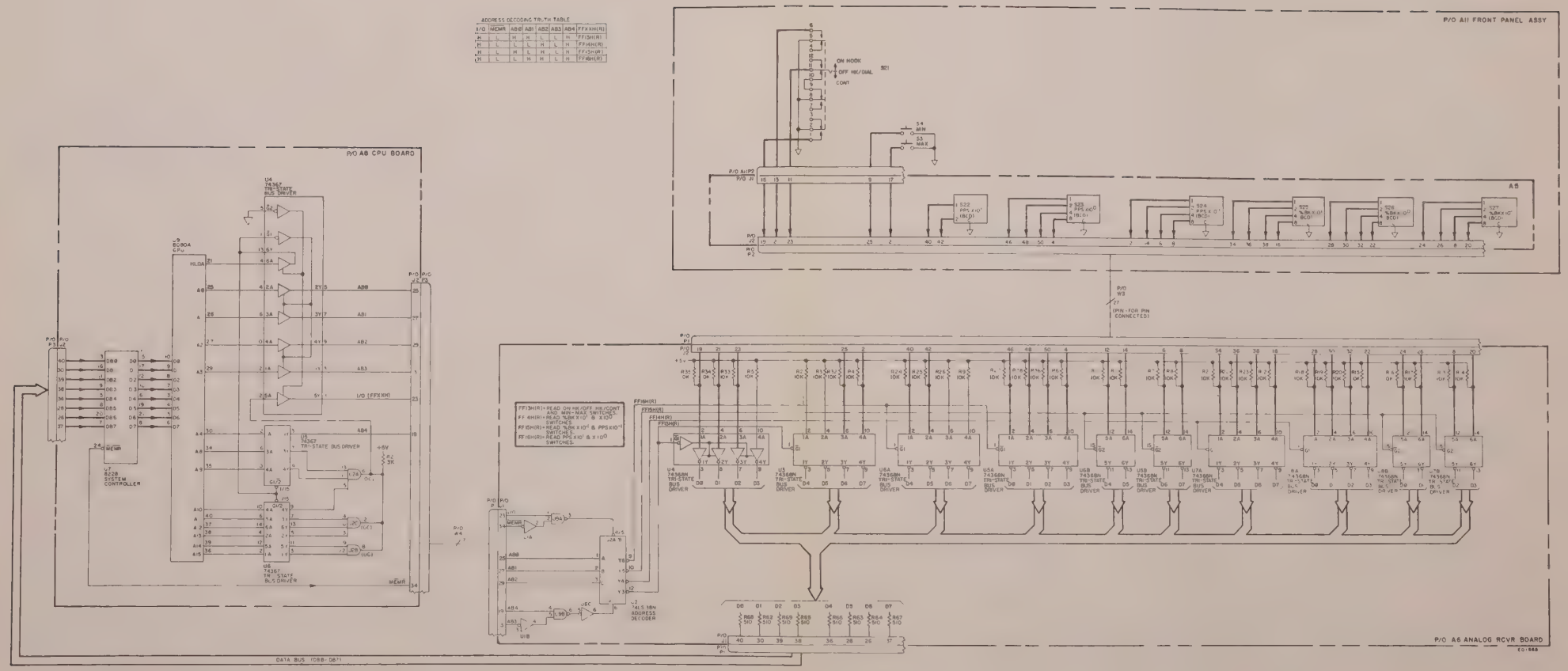


Figure 7—5. Switch Status Functional Schematic Diagram

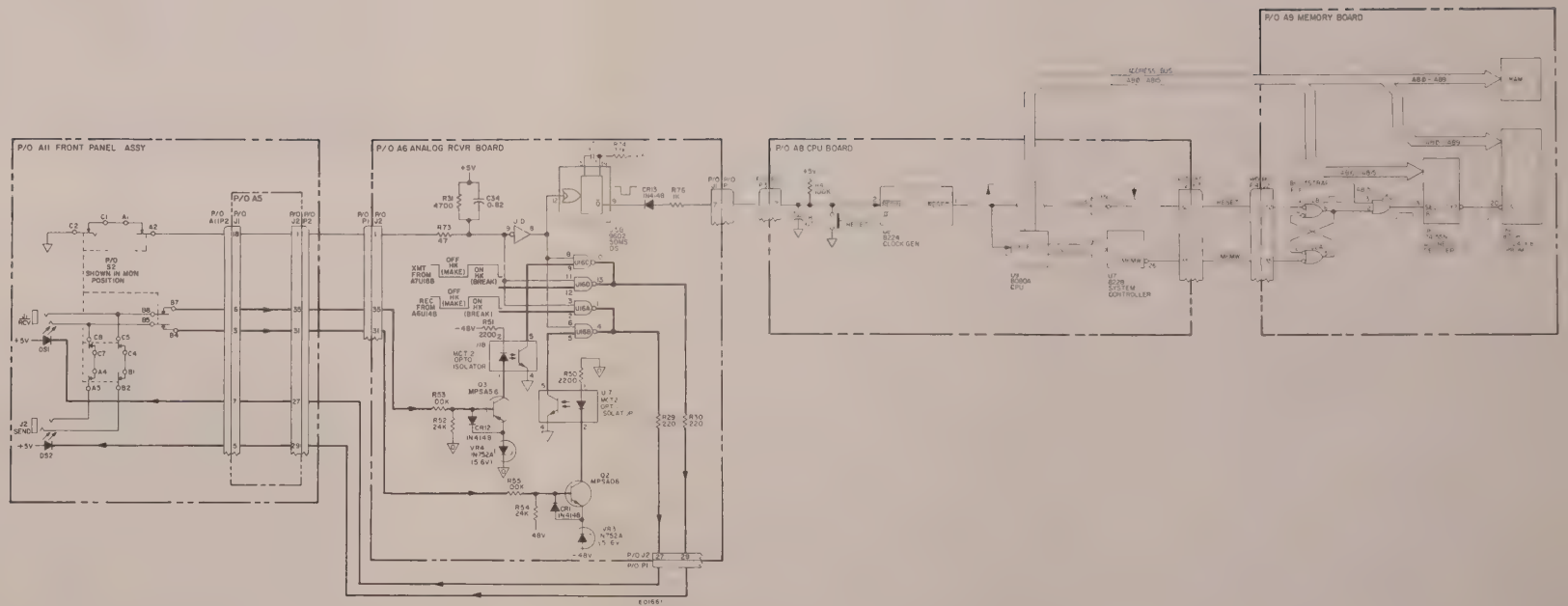


Figure 7—6. Reset And Monitor Functional Schematic Diagram

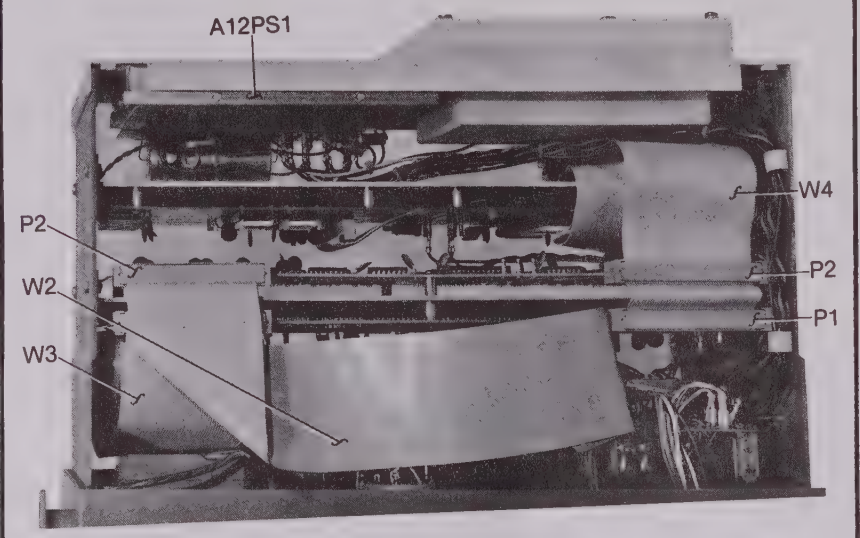


Figure 7—7. Location Of The Main Interconnecting Cables

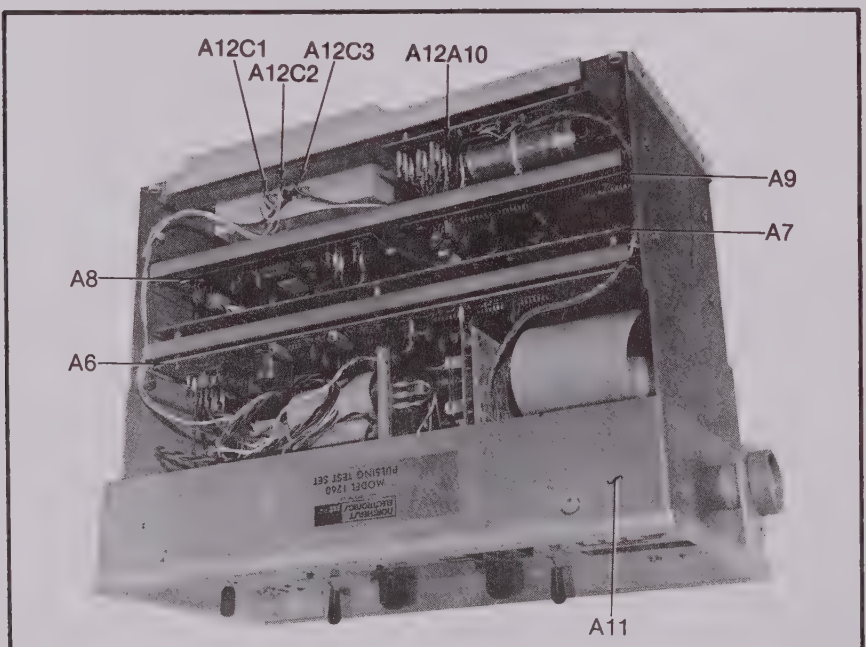


Figure 7—8. Location Of Subassemblies

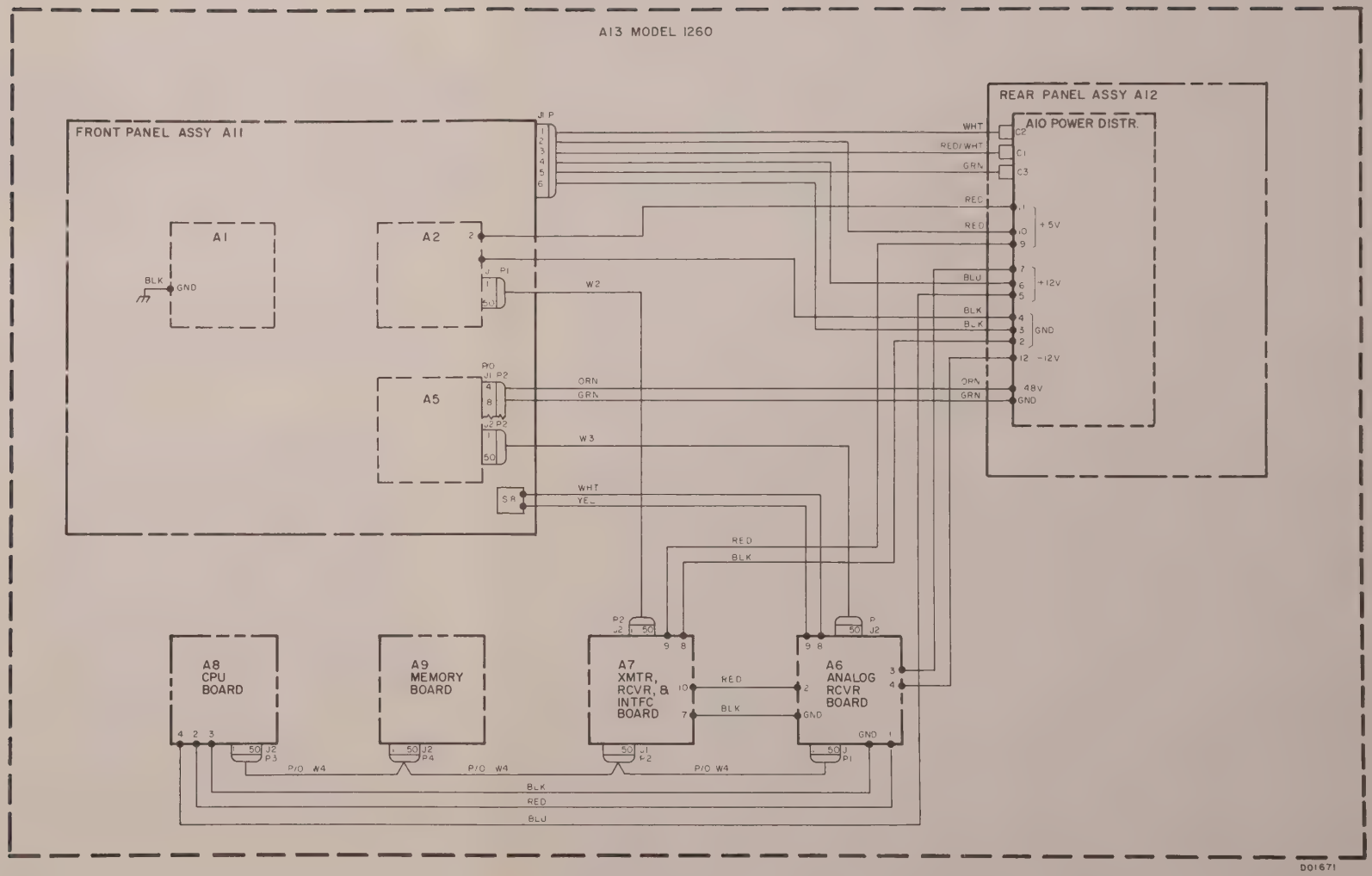


Figure 7—9. Overall Cabling Diagram

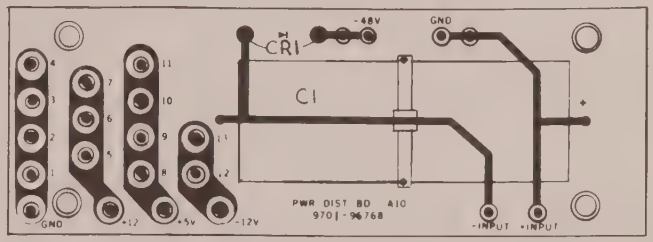


Figure 7—10. Power Distribution Assembly A12A10, Component Location Diagram

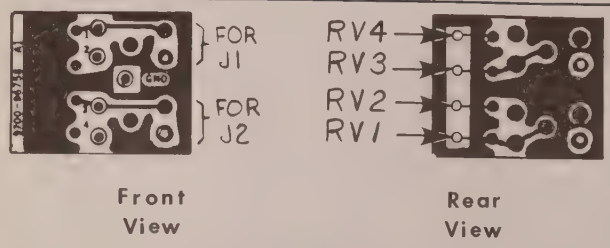


Figure 7—11, Suppressor Assembly A11A1, Component Location Diagram

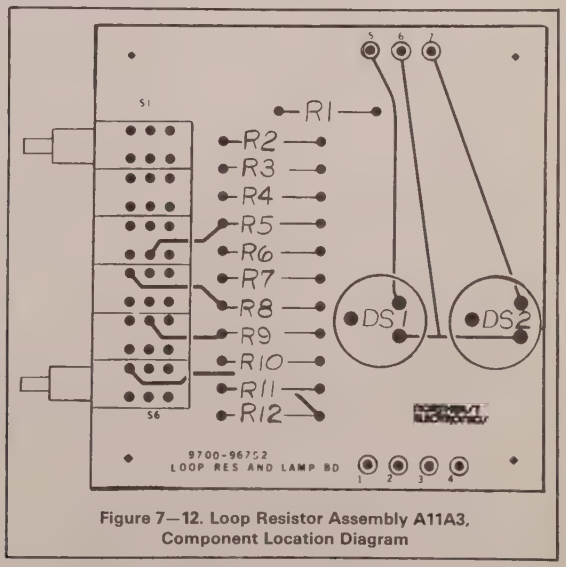


Figure 7—12. Loop Resistor Assembly A11A3, Component Location Diagram

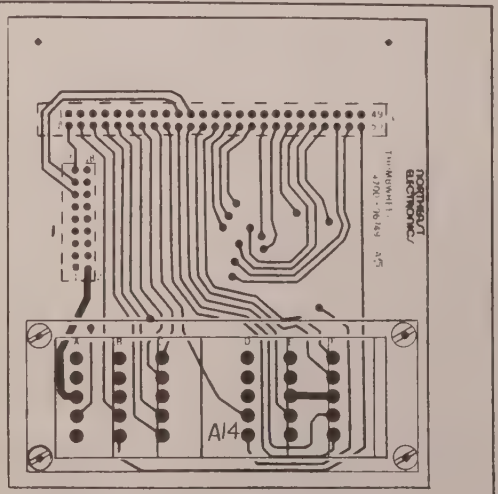


Figure 7—13. Percent Break And Pulse Speed Switch Assembly A11A5, Component Location Diagram

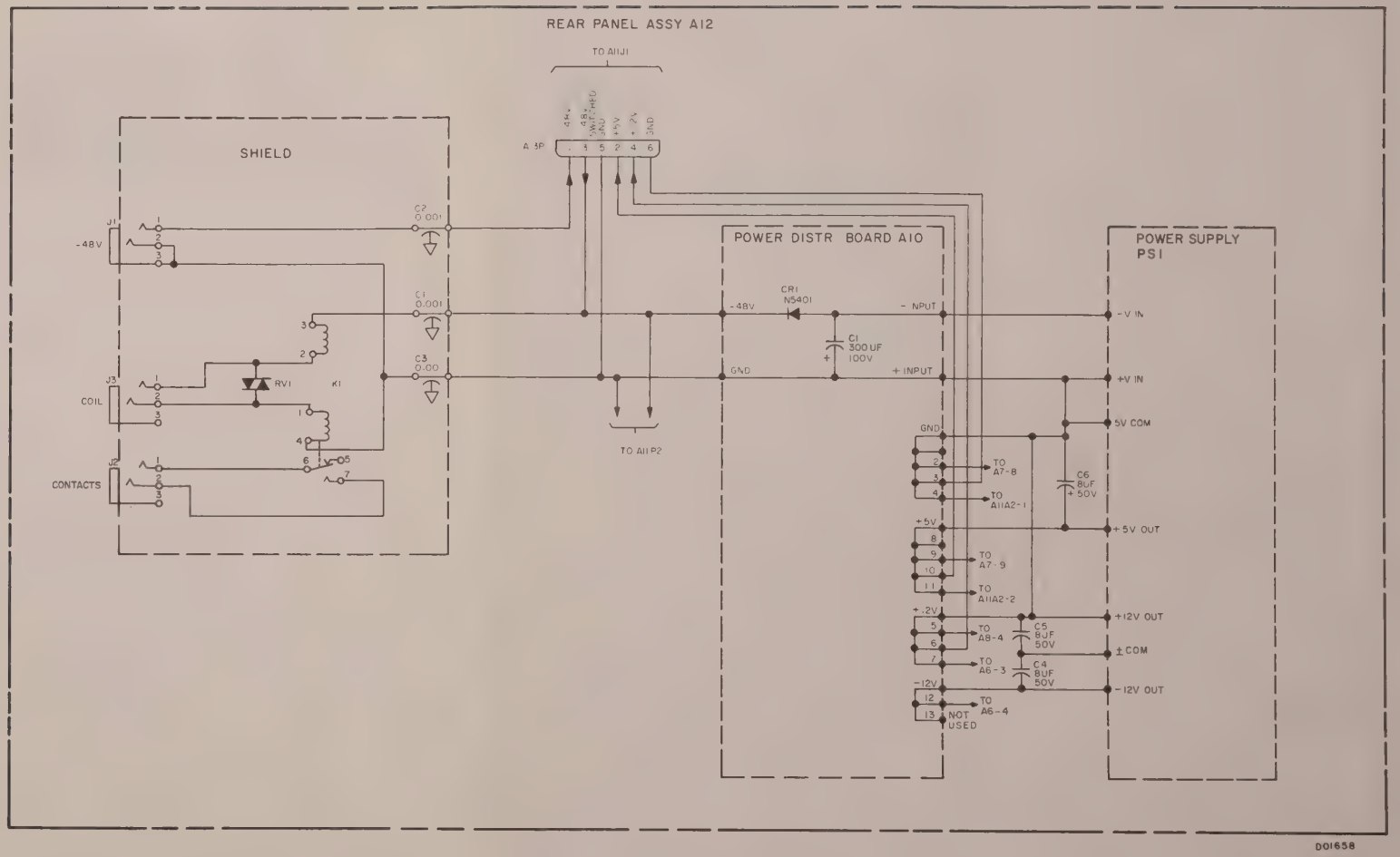


Figure 7—14. Rear Panel Assembly A12, Schematic Diagram

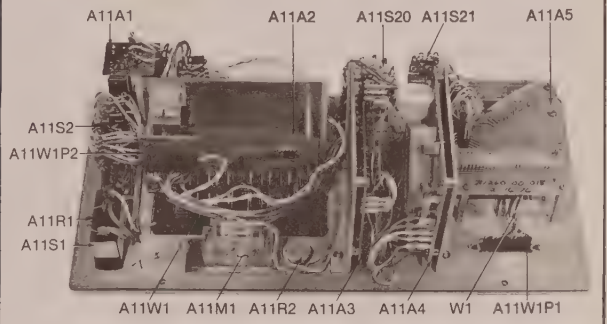


Figure 7—15. Front Panel Assembly A11, Top View, Component Location Diagram

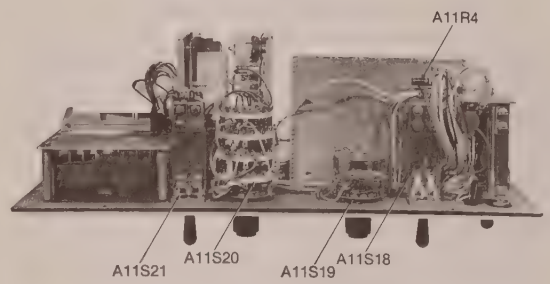


Figure 7—16. Front Panel Assembly A11, Bottom View, Component Location Diagram

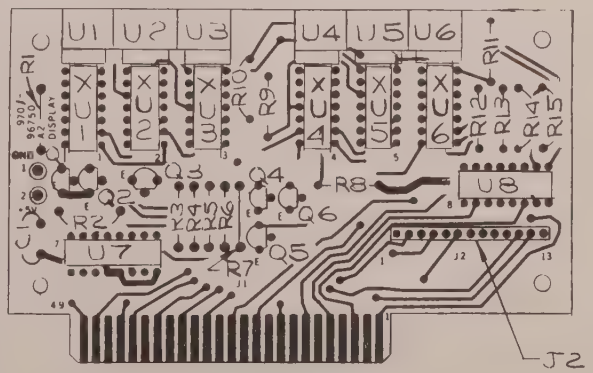


Figure 7—17. Display Assembly A11A2, Component Location Diagram

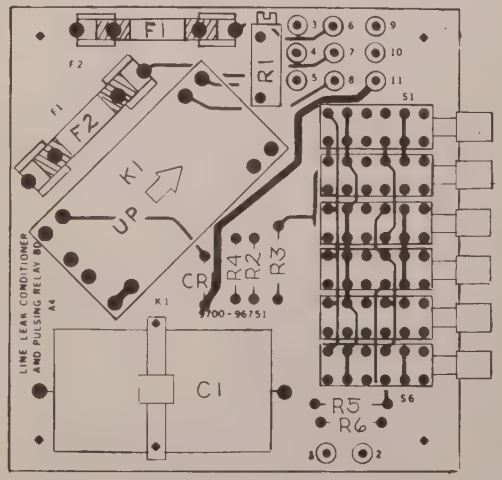


Figure 7—18. Leak Assembly A11A4, Component Location Diagram

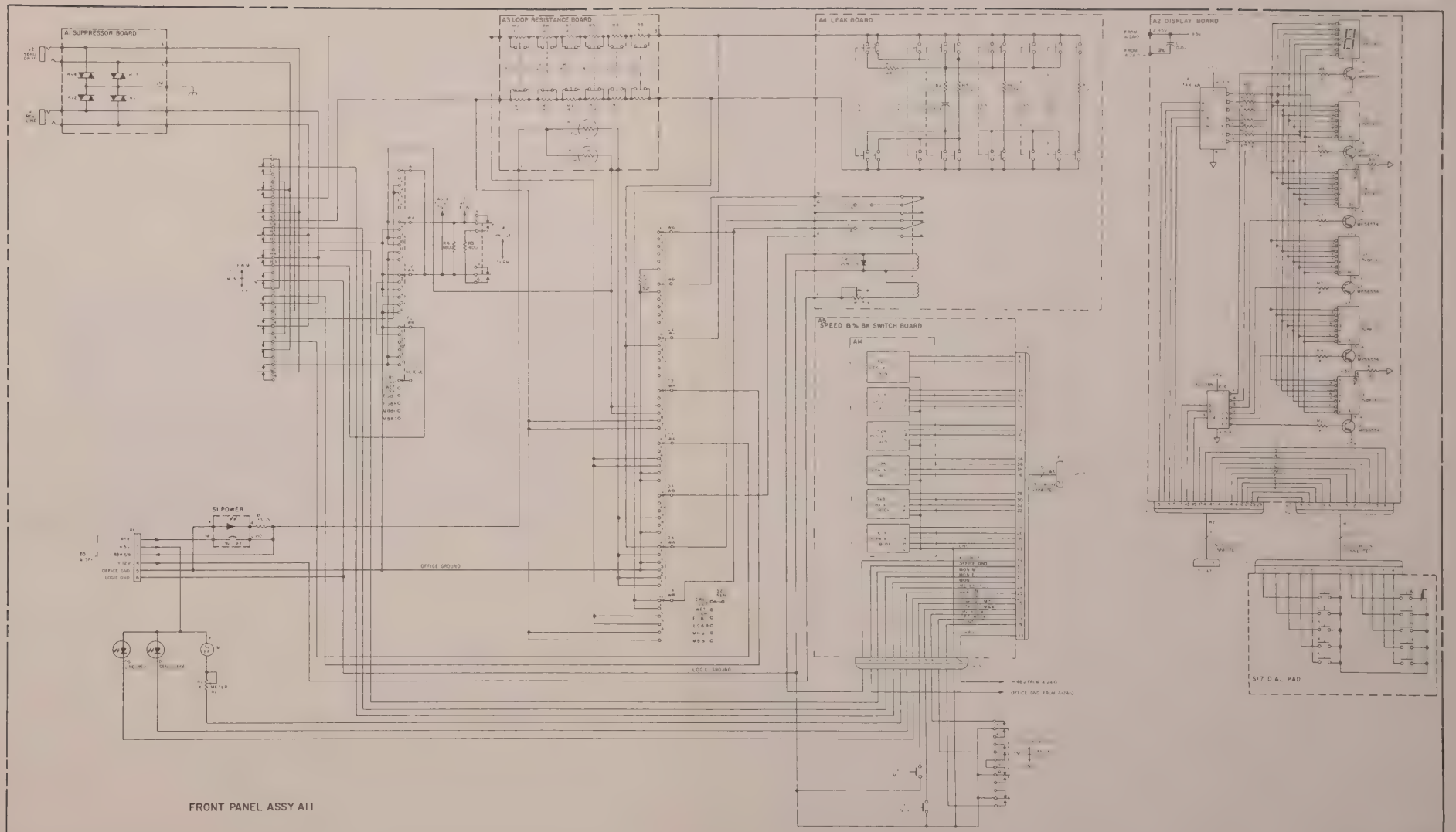


Figure 7—19. Front Panel Assembly A11, Schematic Diagram

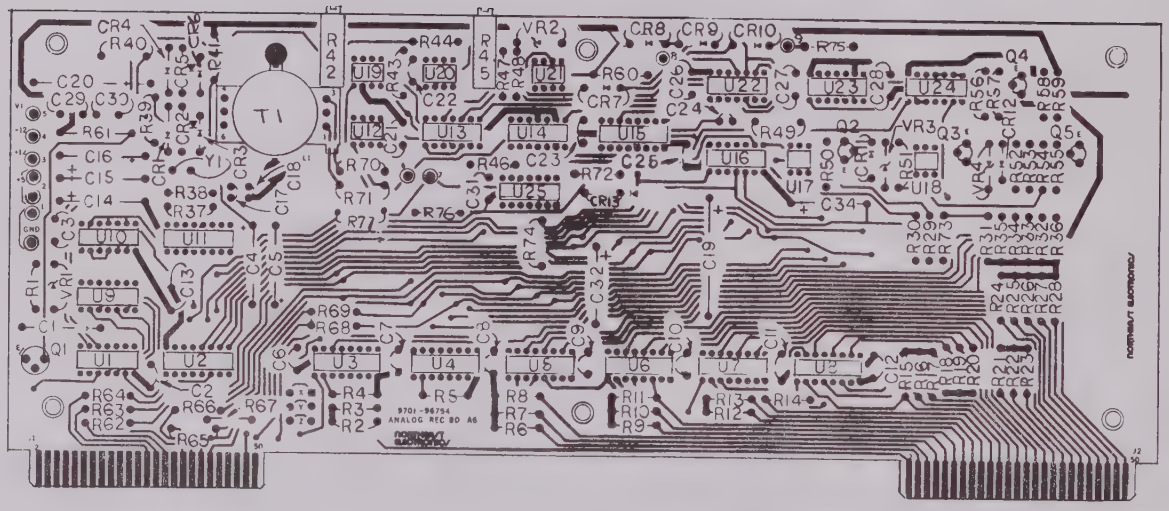


Figure 7—20. Analog Receiver Assembly A6, Component Location Diagram

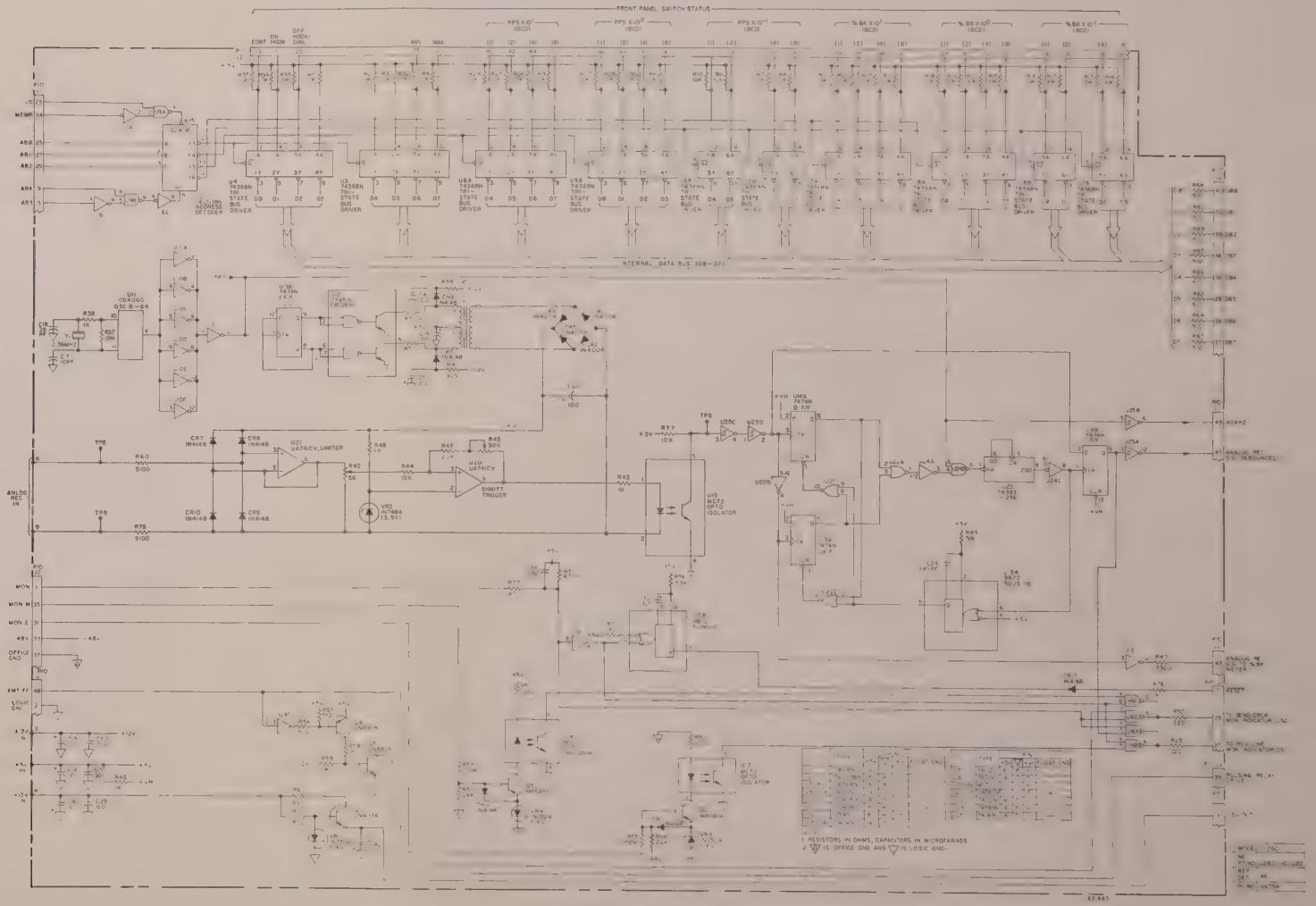


Figure 7—21. Analog Receiver Assembly A6, Schematic Diagram

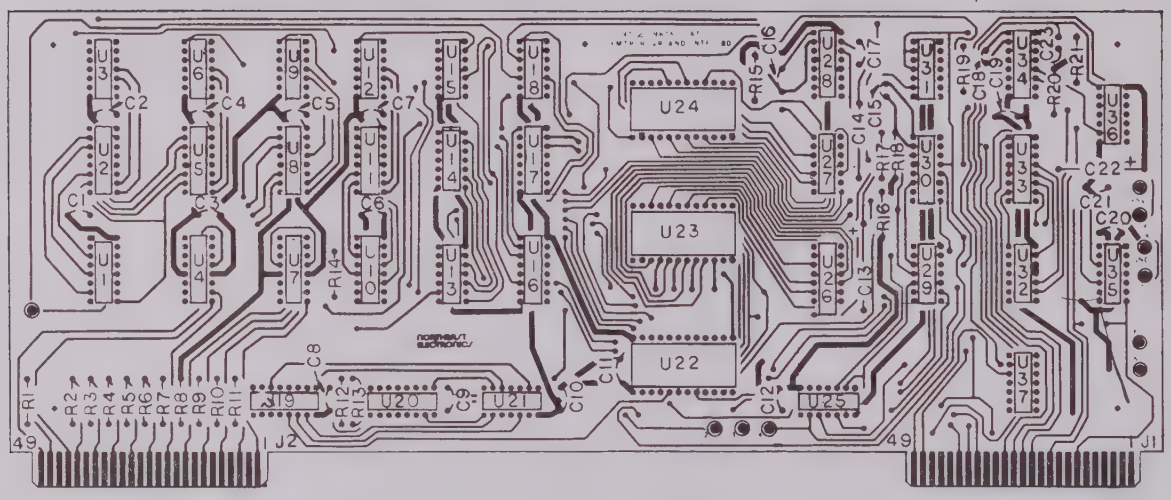


Figure 7—22. Transmitter, Receiver, And Interface Assembly A7, Component Location Diagram

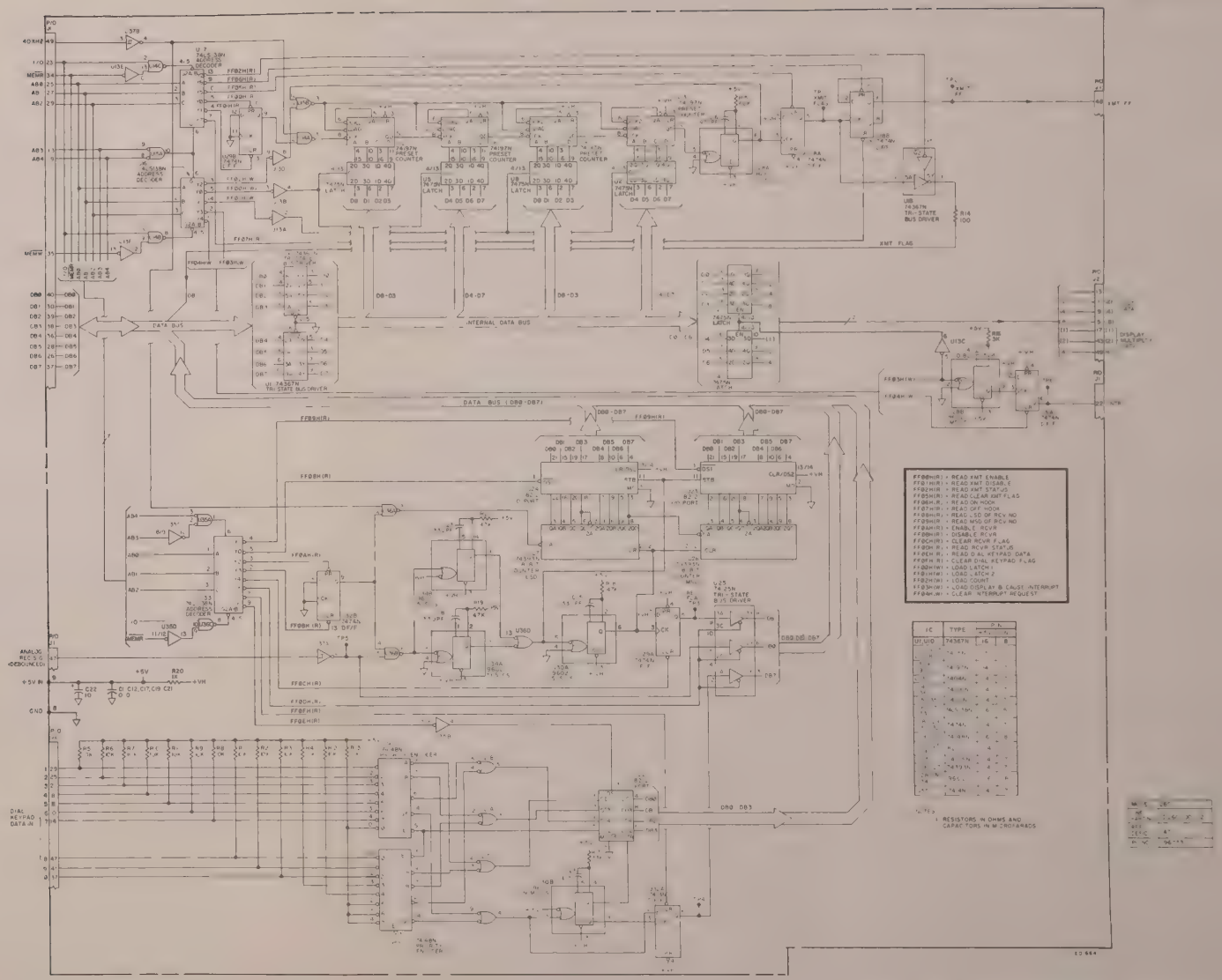


Figure 7—23. Transmitter, Receiver, And Interface Assembly A7, Schematic Diagram

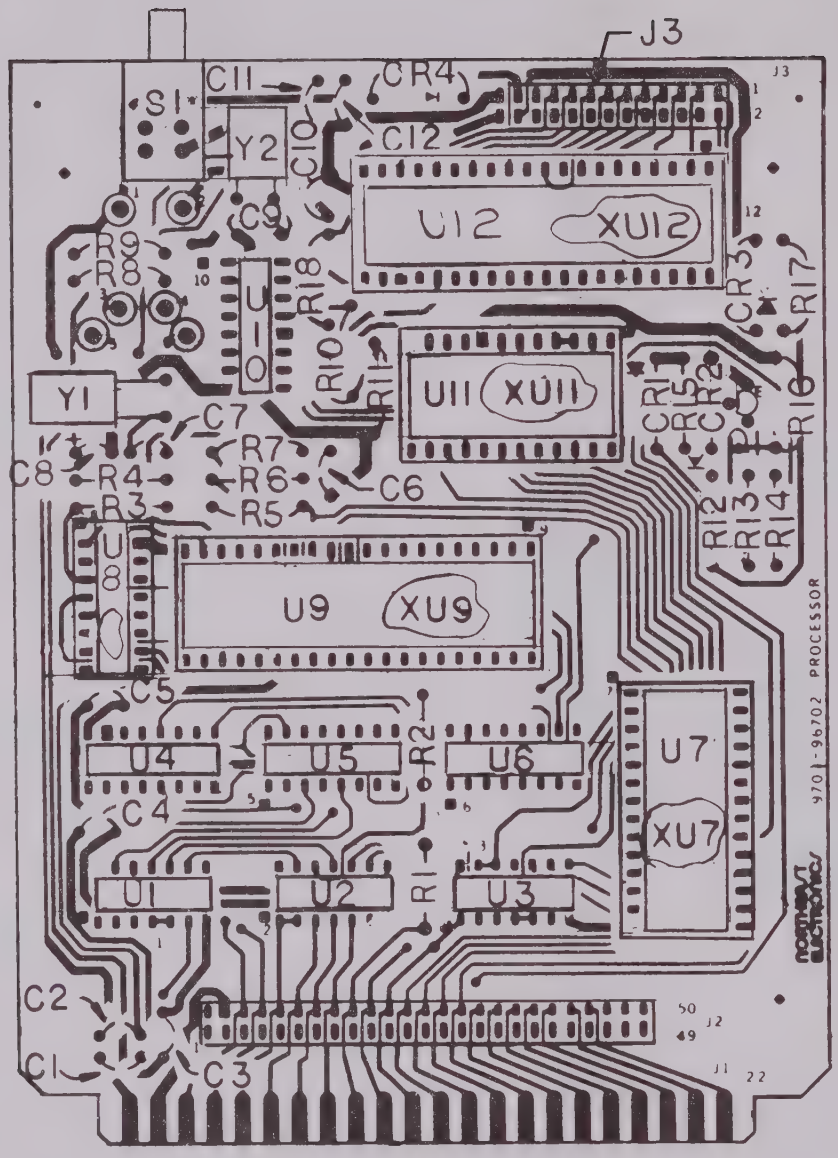
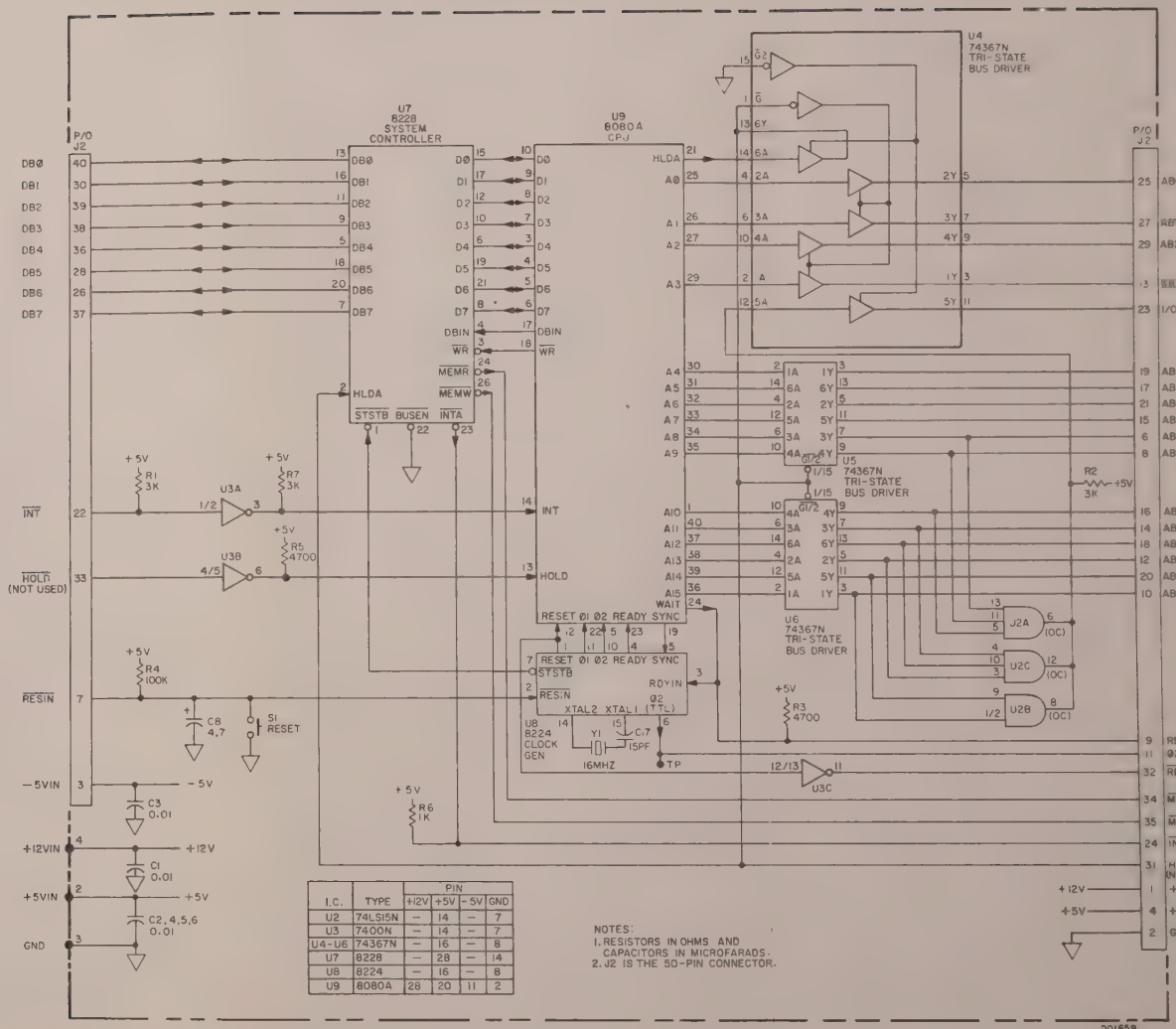


Figure 7—24. CPU Assembly A8, Component Location Diagram



I.C.	TYPE	PIN			
		+12V	+5V	-5V	GND
U2	74LS15N	–	14	–	7
U3	7400N	–	14	–	7
U4-U6	74367N	–	16	–	8
U7	8228	–	28	–	14
U8	8224	–	16	–	8
U9	8080A	28	20	11	2

NOTES:
1. RESISTORS IN OHMS AND CAPACITORS IN MICROFARADS.
2. J2 IS THE 50-PIN CONNECTOR.

MODEL 1260	
NE PART NO.	01260-00-078
REF DESIG	A8
P.C.NO.	96702

Figure 7—25. CPU Assembly A8, Schematic Diagram

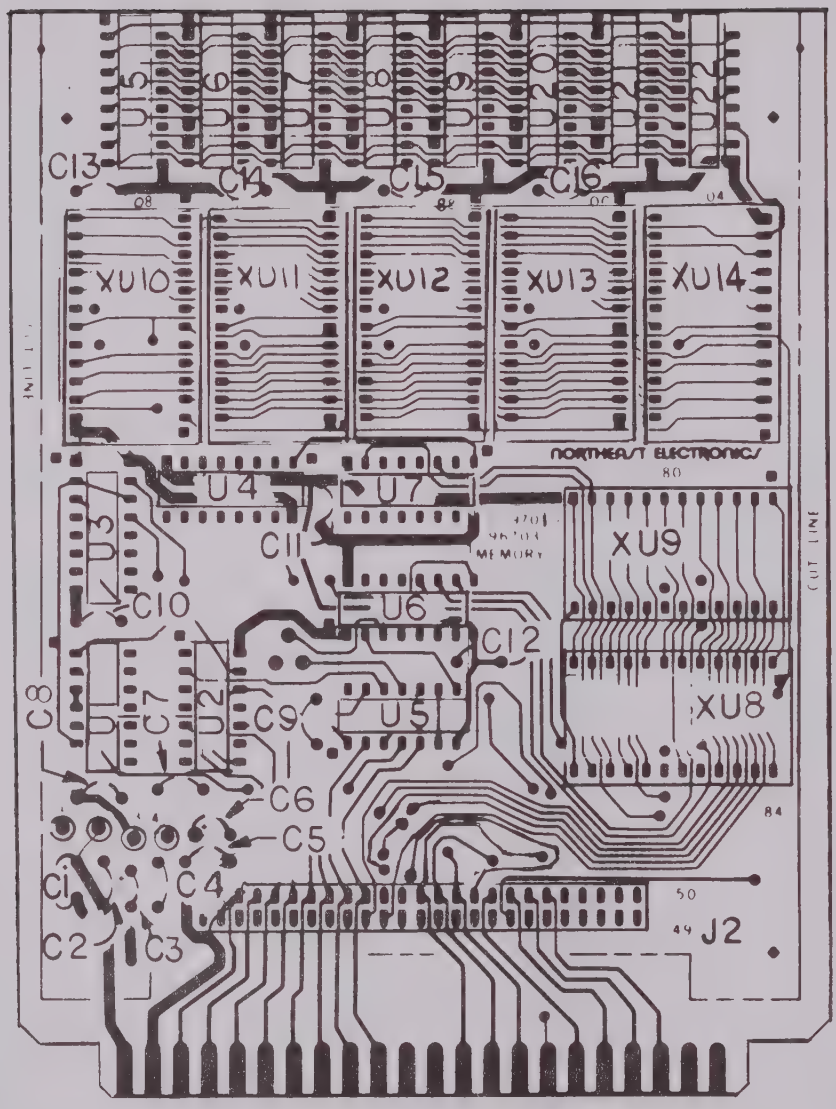


Figure 7—26. Memory Assembly A9, Component Location Diagram

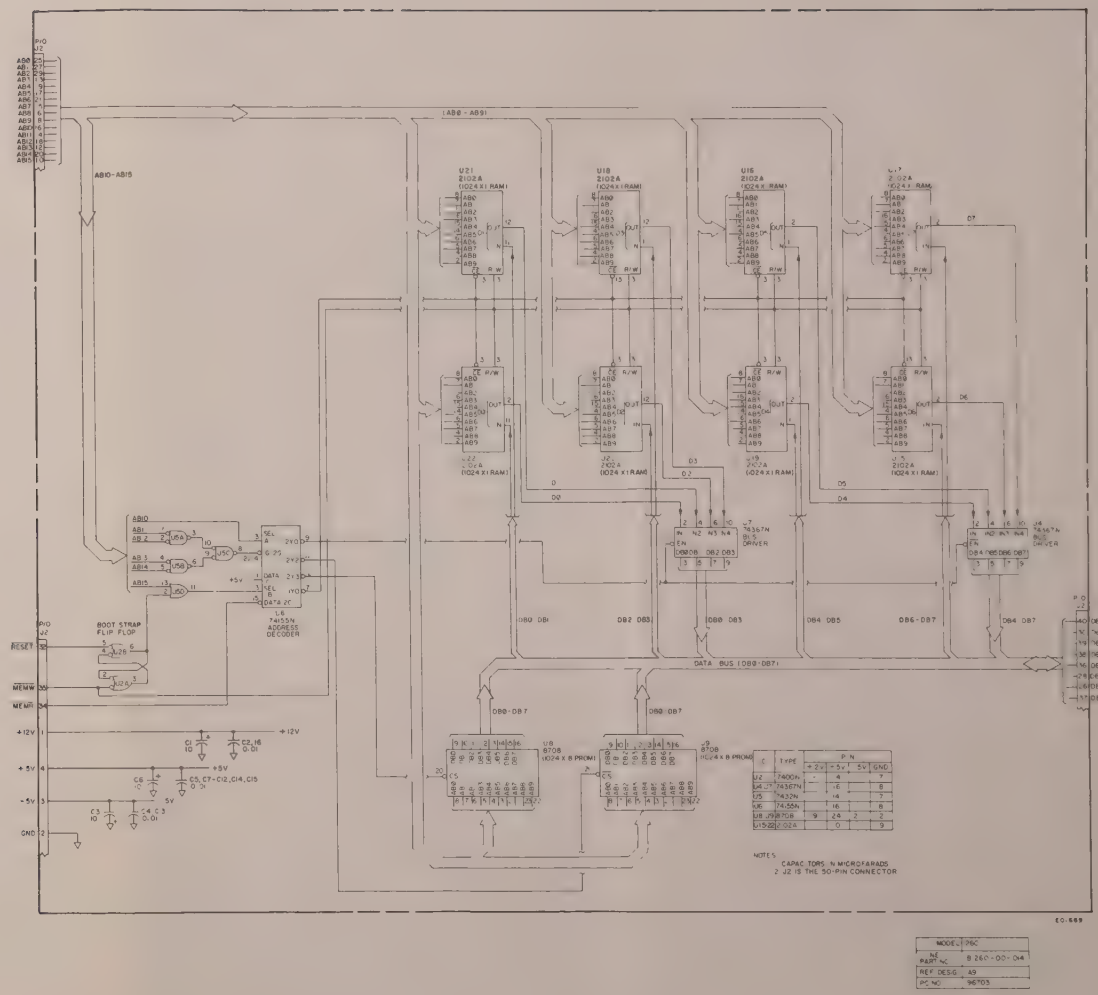


Figure 7–27. Memory Assembly A9, Schematic Diagram

SECTION 8

ELECTRONIC PARTS LISTS

8.1 This section contains the electronic parts lists for the Model 1260.

Table 8—1. Model 1260 Overall Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A6	ANALOG REC 96754 A6						A126000022
A7	XMIT-REC INTF 96753 A7						A126000021
A8	BASIC BMSC PROCESSOR BD						A000100078
A9	BMSC MEMORY A9						A126000014
A11	FRONT PANEL ASSY						A126000024
A12	REAR PANEL ASSY						A126000025
J1	6 COND				AMP	1-480270-0	650800200
W2	DISPLAY CABLE W2						A126000012
W3	THUMBWHEEL CABLE W3						A126000013
W4	CPU CABLE W4						A126000023

Table 8—2. Rear Panel Assembly A12 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A10	POWER DISTR 96768 A10						A126000020
C1-3	.001UF		20%	500V	ERIE	357-001-X5U0-102M	331101020
C4-6	8UF			50V	SPRAGUE	TE-1303.3	300208051
J1-3	MT332B				SWCRFT	5J-1583	650403100
K1	IC PC 2-.2K A-RELAY				AE	PR-1610-A4	600300100
PS1	5V-3A +-12V- .33				S.-ARNOLD	S48/T12/330V	960100001
RV1	VARISTOR MET OXIDE				GE	V250LA4	565500250

Table 8—3. Power Distribution Assembly A12A10 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	300UF			100V	SPRAGUE	34D307F100JP4	301403071
CR1	A3Q	3A	SI	100V	WSTNGHOUSE	1N5401	560054010

Table 8—4. Front Panel Assembly A11 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A1	SUPPRESSOR BD 96758 A1						A126000015
A2	DISPLAY BD 96750 A2						A126000016
A3	LOOP RES.&LAMP 96752 A3						A126000017
A4	LINE LEAK 96751 A4						A126000019
A5	THUMBWHEEL 96749 A5						A126000018
DS1-2		20 MA			H.PACKARD	5082-4655	564500802
J1-2	CKT 4 A FRAME				SWCRFT	5J-1597	650403700
M1		1 MA			MODUTEC	MED MA 001	900000001
P1	6 COND				AMP	1-480271-0	550800100
R1	3.3K	1/2W	5%		AB	TYPE EB	200203325
R2	1K	.25W	20%	LIN	CRL	JC-102	238201020
R3	400-	25W	1%		DALE	RH-25	210904011
R4	6.8K	1W	10%		AB	TYPE GB	200306826
S1		2.5 A			AIRPAX	203-2-1-52-252-5-1-8	862901201
S2	3C-2C-3C-2C				STROMBERG	200150-433	530100104
S3-4	SPST				GREYHILL	30-3	635500201
S17	12 BUTTON KEYPAD				DIGITRAN	KL 0025	535000300
S18	SWITCH,LEVER,1C-1C-0-0				SWITCHCRFT	6006L	630600600
S19	RECEIVE SWITCH ASSY S19						A126000026
S20	SEND SWITCH ASSY S20						A126000027
S21	SW,LEVER,2C-2C				SWCRFT	60312L	630600400
W1	KEYPAD CABLE W1						A126000032

Table 8—5. Suppressor Assembly A11A1 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
RV1-4	VARISTOR,MET OXIDE				GE	V95LA7A	565500201

Table 8—6. Display Assembly A11A2 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	.01UF		00	50V	CENTRALAB	CK-103	330701030
J2	13 SIL				BERG	65500-113	654003423
Q1-6	TO92 310MW TC PNP			40V	MOTOROLA	MPS6534	552065340
R1	120-	1/4W	10%		AB	TYPE CB	200101216
R2-7	1K	1/4W	10%		AB	TYPE CB	200101026
R8-15	120-	1/4W	10%		AB	TYPE CB	200101216
U1-6	14PDIL	20MA	RED		HP	5082-7650	728301701
U7	16 DIP-P			LS	TI	SN74LS138N	510974138
U8	16DIP-P			TTL	T.I.	SN7447AN	510074470
XU1-6	14 DIP RIGHT ANGLE SOCKET				ARIES	14-810-90	820101710

Table 8—7. Loop Resistor Assembly A11A3 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R1	50-	3W	1%		TEL LABS	EL2B	210350091
R2	100-	3W	1%		TEL LABS	EL2B	210310001
R3	50-	3W	1%		TEL LABS	EL2B	210350091
R4	100-	3W	1%		TEL LABS	EL2B	210310001
R5-6	200-	3W	1%		TEL LAB	EL-2B	210320001
R7	400-	3W	1%		TEL LAB	EL2B	210340001
R8	800-	3W	1%		TEL LAB	EL2B	210380001
R9	400-	3W	1%		TEL LAB	EL2B	210340001
R10	800-	3W	1%		TEL LAB	EL2B	210380001
R11-12	1600-	3W	1%		TEL LABS	EL2B	210316011
RT1-2	MINI GB-13A,9 PIN TUB.SKT				SYLVANIA	GB-19A	730100101

Table 8—8. Percent Break And Pulse Speed Switch Assembly A11A5 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A14	BLACK				DIGITRAN	29N12	626800902
J1	9 DIL				BERG	65610-118	654003327
J2	50PIN				3M CO.	3433-2003	654000400

Table 8—9. Leak Assembly A11A4 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	2.16UF		2%	400V	N.TELECOM	CM01Y-2.16UFG400	335321640
CR1	DO41	1A	SI	400V	EDAL	IN4004	560040040
F1-2		1A		250V	LITTELFUSE	3AG	863100400
K1	RELAY,MERC.WET,PC	2C	BIPL		MIDTEX	161-262NA1	604104501
R1	500-	.75W	10		HELIPOT	89PR500	232505010
R2	4420-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220244211
R3	10.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210221
R4	600-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260001
R5	15K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215021
R6	20.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220521

Table 8—10. Receive Switch Assembly S19 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
S19		1A		28V	OAK	399429K	626301800

Table 8—11. Send Switch Assembly S20 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
R1	1K	1W	10%		AB	TYPE GB	200301026
S20		1A		28V	OAK	269720-J4C	626200200

Table 8—12. Keypad Cable A11W1 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
P1-2	13 SIL				BERG	65039-024	652002023

Table 8—13. Analog Receiver Assembly A6 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
C1	.82UF		10%	35V	SPRAGUE	150D824X9035A2	310308240
C2-3	.01UF		00	50V	CENTRALAB	CK-103	330701030
C4-5	2.2UF	B	10%	35V	SPRAGUE	196D225X9035JA1	310802250
C6-13	.01UF		00	50V	CENTRALAB	CK-103	330701030
C14-16	10UF		10%	20V	SPRAGUE	150D106X9020B2	310301060
C17	10PF DA	N330	10%	1KV	CENTRALAB	DD-100	330001000
C18	39PF DA	N330	10%	1KV	CENTRALAB	DD-390	330003900
C19-20	100UF	F	10%	10V	SPRAGUE	196D107X9010PE4	310801070
C21-23	.01UF		00	50V	CENTRALAB	CK-103	330701030
C24	330PF DB	Z5F	10%	1KV	CENTRALAB	DD-331	330003310
C25-31	.01UF		00	50V	CENTRALAB	CK-103	330701030
C32	4.7UF	B	20%	35V	SPRAGUE	196D475X0035JA1	310804750
C34	.82UF		10%	35V	SPRAGUE	150D824X9035A2	310308240
CR1-2	D041	1A	SI	400V	EDAL	IN4004	560040040
CR3	D035 4NS	10MA	SI	50UA	FAIRCHILD	IN4148	560041480
CR4-5	D041	1A	SI	400V	EDAL	IN4004	560040040
CR6-13	D035 4NS	10MA	SI	50UA	FAIRCHILD	IN4148	560041480
Q1	TO5 7W	TA	PNP	65V	RCA	2N4036	552040360
Q2	TO-92 625MW	TA	NPN	80V	MOTOROLA	MPS-A06	550000060
Q3	TO92 625MW	TA	PNP	80V	MOTOROLA	MPS A-56	552000560
Q4	TO92 350MW	TC	PNP	40V	MOTOROLA	2N3905	552039050
Q5	TO-92 350MW	TA	NPN	40V	MOTOROLA	2N3903	550039030
R1	820-	1/4W	10%		AB	TYPE CB	200108216
R2-28	10K	1/4W	10%		AB	TYPE CB	200101035
R29-30	220-	1/4W	10%		AB	TYPE CB	200102216
R31	4.7K	1/4W	10%		AB	TYPE CB	200104726
R32-36	10K	1/4W	10%		AB	TYPE CB	200101036
R37	10M	1/4W	10%		AB	TYPE CB	200101066
R38	1K	1/4W	10%		AB	TYPE CB	200101026
R39	100-	1/4W	10%		AB	TYPE CB	200101016
R40	3.3K	1/4W	10%		AB	TYPE CB	200103326
R41	100-	1/4W	10%		AB	TYPE CB	200101016
R42	5K	.75W	10		HELIPOT	89PR5K	232505020
R43	1K	1/4W	10%		AB	TYPE CB	200101026
R44	10K	1/4W	10%		AB	TYPE CB	200101036
R45	50K	.75W	10		HELIPOT	89PR50K	232505030
R46	1K	1/4W	10%		AB	TYPE CB	200101025
R47	20K	1/4W	10%		AB	TYPE CB	200102036
R48	1K	1/4W	10%		AB	TYPE CB	200101026

Table 8—13. (cont'd)

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
R49	51K	1/4W	10%		AB	TYPE CB	200105136
R50-51	2.2K	1/4W	10%		AB	TYPE CB	200102226
R52	24K	1/4W	5%		AB	TYPE CB	200102435
R53	100K	1/4W	10%		AB	TYPE CB	200101046
R54	24K	1/4W	5%		AB	TYPE CB	200102435
R55	100K	1/4W	10%		AB	TYPE CB	200101046
R56-57	510-	1/4W	5%		AB	TYPE CB	200105115
R58-59	1K	1/4W	10%		AB	TYPE CB	200101026
R60	5.1K	1/2W	5%		AB	TYPE EB	200205125
R61	62-	1W	10%		A.B.	TYPE GB	200306206
R62-69	510-	1/4W	5%		AB	TYPE CB	200105115
R70-71	10-	1/4W	10%		AB	TYPE CB	200101006
R72	1K	1/4W	10%		AB	TYPE CB	200101026
R73	47-	1/4W	10%		AB	TYPE CB	200104706
R74	33K	1/4W	10%		AB	TYPE CB	200103336
R75	5.1K	1/2W	5%		AB	TYPE EB	200205125
R76	1K	1/4W	10%		AB	TYPE CB	200101026
R77	10K	1/4W	10%		AB	TYPE CB	200101036
T1	TRANSFORMER,POT-CORE				ARTTED	9311	420900101
U1	14DIP-P			TTL	TI	SN7404N	510074040
U2	16 DIP-P			LS	TI	SN74LS138N	510974138
U3-8	16DIP-P			TTL	TI	SN74368N	510074368
U9	14DIP-P			TTL	TI	SN7400N	510074000
U10	14DIP-P	B		CMOS	RCA	CD4069	510004069
U11	16DIP-P	B		CMOS	RCA	CD4060	510004060
U12	8DIP-P			DS	TI	SN75451BP	510075451
U13-14	14DIP-P			TTL	TI	SN7474N	510074740
U15	16DIP-P			DM3	FAIRCHILD	9602PC	510096025
U16	14DIP-P			TTL	TI	SN7401N	510074010
U17-19	6PDIL	250MW			MONSANTO	MCT2	515000200
U20-21	8PDIL	00MW		180	SIGNETICS	UA741CV	500057410
U22	14DIP-P			TTL	TI	SN7402N	510074020
U23	14DIP-P			TTL	TI	SN74393N	510074393
U24	14DIP-P			TTL	TI	SN7400N	510074000
U25	14DIP-P			TTL	TI	SN7414N	510007414
VR1	A1	400MW	5%	5.6V	DICKSON	1N752A	562007520
VR2	A1	400MW	5%	3.9V	TI	1N748A	562007481
VR3-4	A1	400MW	5%	5.6V	DICKSON	1N752A	562007520
Y1	PAR RES. 500 OHMS				INTERNAT'L	HC-18, 2.56MHZ	919100002

Table 8—14. Transmitter, Receiver, And Interface Assembly A7 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-12	.01UF		00	50V	CENTRALAB	CK-103	330701030
C13	4.7UF	B	20%	35V	SPRAGUE	196D475X0035JA1	310804750
C14	.82UF		10%	35V	SPRAGUE	150D824X9035A2	310308240
C15	330PF DB	Z5F	10%	1KV	CENTRALAB	DD-331	330003310
C16	470PF DB	Z5F	10%	1KV	CENTRALAB	DD-471	330004710
C17	.01UF		00	50V	CENTRALAB	CK-103	330701030
C18	330PF DB	Z5F	10%	1KV	CENTRALAB	DD-331	330003310
C19-21	.01UF		00	50V	CENTRALAB	CK-103	330701030
C22	10UF		10%	20V	SPRAGUE	150D106X9020B2	310301060
C23	330PF DB	Z5F	10%	1KV	CENTRALAB	DD-331	330003310
R1-13	10K	1/4W	10%		AB	TYPE CB	200101036
R14	100-	1/4W	10%		AB	TYPE CB	200101016
R15	62K	1/4W	10%		A.B.	TYPE CB	200106236
R16	3K	1/4W	5%		AB	TYPE CB	200103025
R17	33K	1/4W	10%		AB	TYPE CB	200103336
R18-19	47K	1/4W	5%		AB	TYPE CB	200104735
R20	1K	1/4W	10%		AB	TYPE CB	200101026
R21	47K	1/4W	5%		AB	TYPE CB	200104735
U1	16DIP-P			TTL	TI	SN74367N	510074367
U2	16DIP-P			TTL	TI	SN7475N	510074750
U3	14DIP-P			TTL	TI	SN74197N	510074197
U4-5	16DIP-P			TTL	TI	SN7475N	510074750
U6	14DIP-P			TTL	TI	SN74197N	510074197
U7-8	16DIP-P			TTL	TI	SN7475N	510074750
U9	14DIP-P			TTL	TI	SN74197N	510074197
U10	16DIP-P			TTL	TI	SN74367N	510074367
U11	16DIP-P			TTL	TI	SN7475N	510074750
U12	14DIP-P			TTL	TI	SN74197N	510074197
U13	14DIP-P			TTL	TI	SN7404N	510074040
U14	14DIP-P		L	TTL	TI	SN74L00N	510074001
U15	14DIP-P			TTL	TI	SN7402N	510074020
U16-17	16 DIP-P			LS	TI	SN74LS138N	510974138
U18	14DIP-P			TTL	TI	SN7474N	510074740
U19-20	16DIP-P			TTL	TI	SN74148N	510074148
U21	14DIP-P		L	TTL	TI	SN74L00N	510074001
U22-24	8 BIT I/O PORT				INTEL	8212	514001500
U25	14DIP-P			TTL	TI	SN74125N	510074125
U26-27	14DIP-P			TTL	TI	SN74393N	510074393
U28	16DIP-P			DM3	FAIRCHILD	9602PC	510096025
U29	14DIP-P			TTL	TI	SN7474N	510074740
U30	16DIP-P			DM3	FAIRCHILD	9602PC	510096025
U31-32	14DIP-P			TTL	TI	SN7474N	510074740
U33	16 DIP-P			LS	TI	SN74LS138N	510974138
U34	16DIP-P			DM3	FAIRCHILD	9602PC	510096025
U35	14DIP-P			TTL	TI	SN7402N	510074020
U36	14DIP-P		L	TTL	TI	SN74L00N	510074001
U37	14DIP-P			TTL	TI	SN7414N	510007414

Table 8—15. CPU Assembly A8 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1-6	.01UF		00	50V	CENTRALAB	CK-103	330701030
C7	15PF DA	N330	10%	1KV	CENTRALAB	DD-150	330001500
C8	4.7UF		10%	25V	KEMET	T330A475K025AS	310004751
J2	25 DIL				BERG	65610-150	654003311
R1-2	3K	1/4W	5%		AB	TYPE CB	200103025
R3	4.7K	1/4W	10%		AB	TYPE CB	200104726
R4	100K	1/4W	10%		AB	TYPE CB	200101046
R5	4.7K	1/4W	10%		AB	TYPE CB	200104726
R6	1K	1/4W	10%		AB	TYPE CB	200101026
R7	3K	1/4W	5%		AB	TYPE CB	200103025
S1	SPDT				CONTROL SW	B8600	635201401
U2	14 DIP-P			LS	TI	SN74LS15N	510907415
U3	14DIP-P			TTL	TI	SN7400N	510074000
U4-6	16DIP-P			TTL	TI	SN74367N	510074367
U7	SYSTEM CONTROLLER				INTEL	8228	514001402
U8	CLOCK GENERATOR				INTEL	8224	514001401
U9	MICRO-PROCESSOR,8 BIT				INTEL	8080A	514001400
XU7	28 DIP				AUGAT	528-AG10D	820101501
XU8	16DIP				AUGAT	516-AG10D	820101703
XU9	40DILP				AUGAT	540-AGID	820101400
Y1	PAR RES. 500 OHMS				INTERNAT'L	HC-18, 16.0MHZ	919100004

Table 8—16. Memory Assembly A9 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
C1	10UF	B	20%	20V	SPRAGUE	196D106X0020JA1	310801060
C2	.01UF		00	50V	CENTRALAB	CK-103	330701030
C3	10UF	B	20%	20V	SPRAGUE	196D106X0020JA1	310801060
C4-5	.01UF		00	50V	CENTRALAB	CK-103	330701030
C6	10UF	B	20%	20V	SPRAGUE	196D106X0020JA1	310801060
C7-16	.01UF		00	50V	CENTRALAB	CK-103	330701030
J2	25 DIL				BERG	65610-150	654003311
U2	14DIP-P			TTL	TI	SN7400N	510074000
U4	16DIP-P			TTL	TI	SN74367N	510074367
U5	14DIP-P			TTL	TI	SN7432N	510074320
U6	16DIP-P			TTL	TI	SN74155N	510074155
U7	16DIP-P			TTL	TI	SN74367N	510074367
U8	1260 PROM#1						B126000030
U9	1260 PROM#2						B126000031
U15-22	RAM,1K X 1				INTEL	2102A	514000401

Table 8—17. Display Cable W2 Parts List

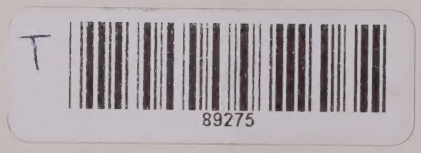
REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
P1-2	2 X 25				3M	3415-0001	654200050

Table 8—18. Pulse Speed And Percent Break Cable W3 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
P1	2 X 25				3M	3415-0001	654200050
P2	50PIN				3M CO	34250000	654000300

Table 8—19. CPU Cable W4 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
P1-2	50PIN				3M CO	34250000	654000300
P3-4	2 X 25				3M	3415-0001	654200050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